BEST AVAILABLE COPY

FIG. 1

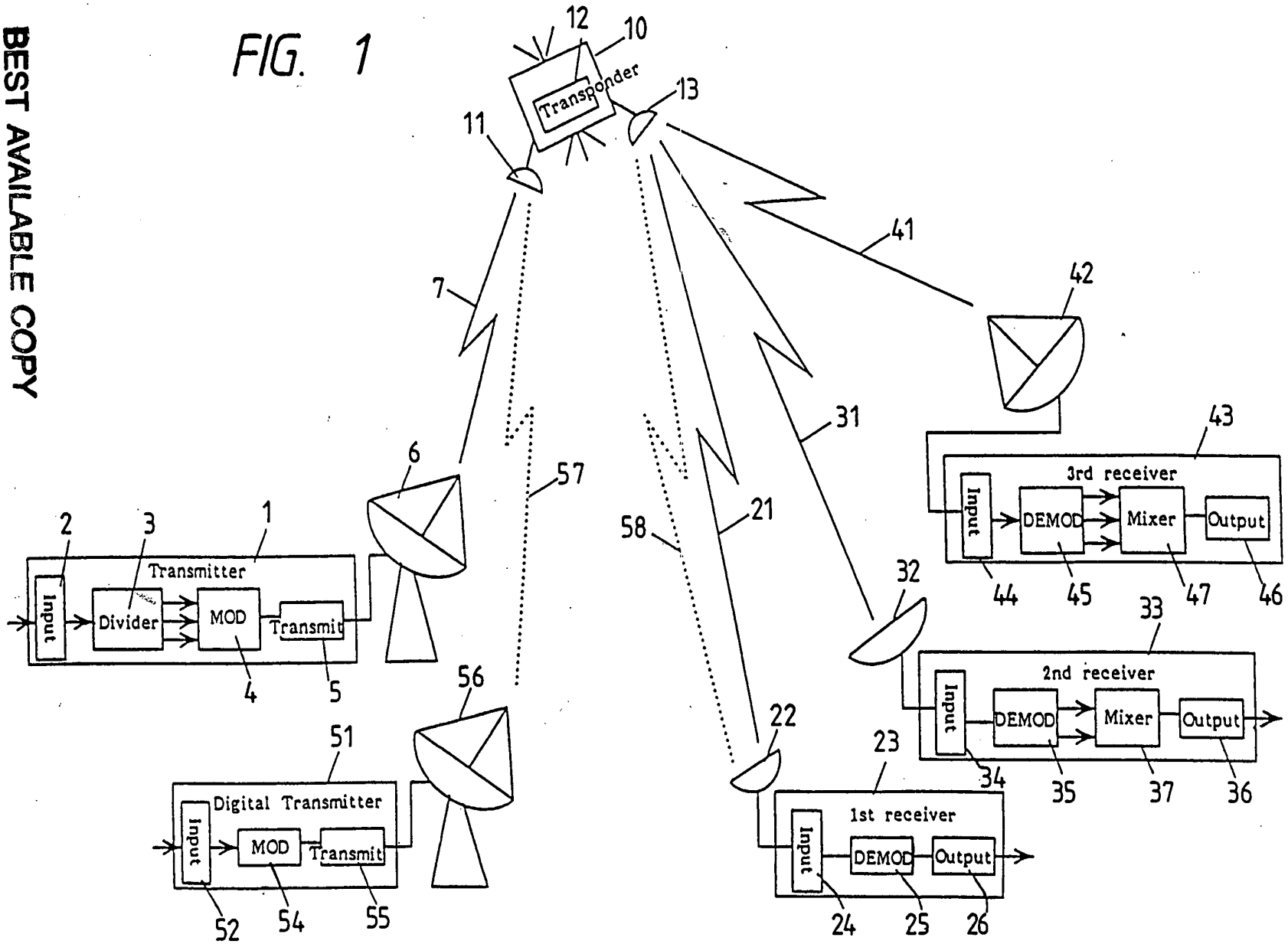


FIG. 2

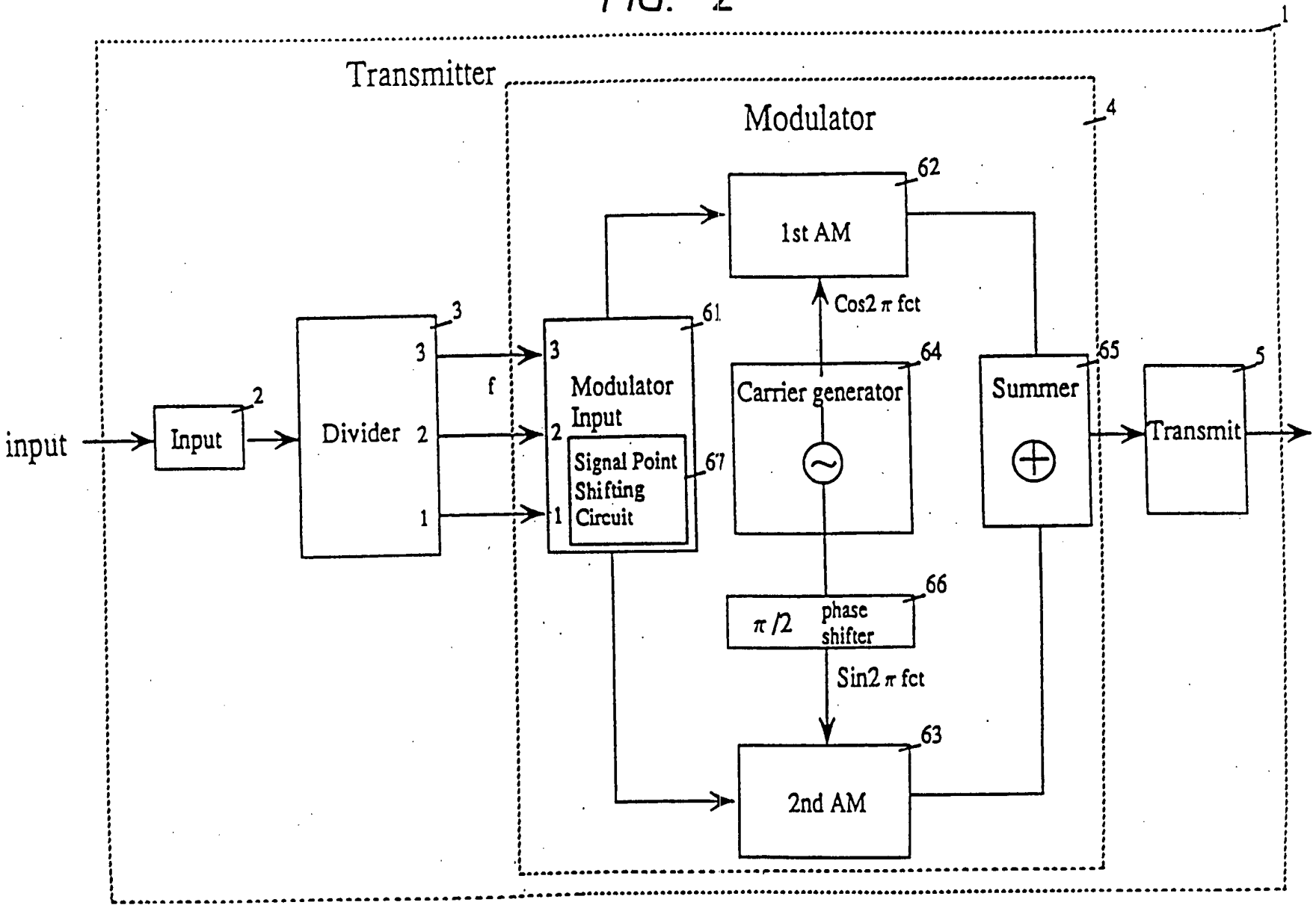

1
Transmitter
Modulator
4
62
1st AM
Cos2 π fct
64
Carrier generator
65
Summer
5
Transmit
input
2
Input
Divider
3
3
2
1
f
61
Modulator Input
Signal Point Shifting Circuit
67
66
π /2 phase shifter
Sin2 π fct
63
2nd AM

FIG. 3

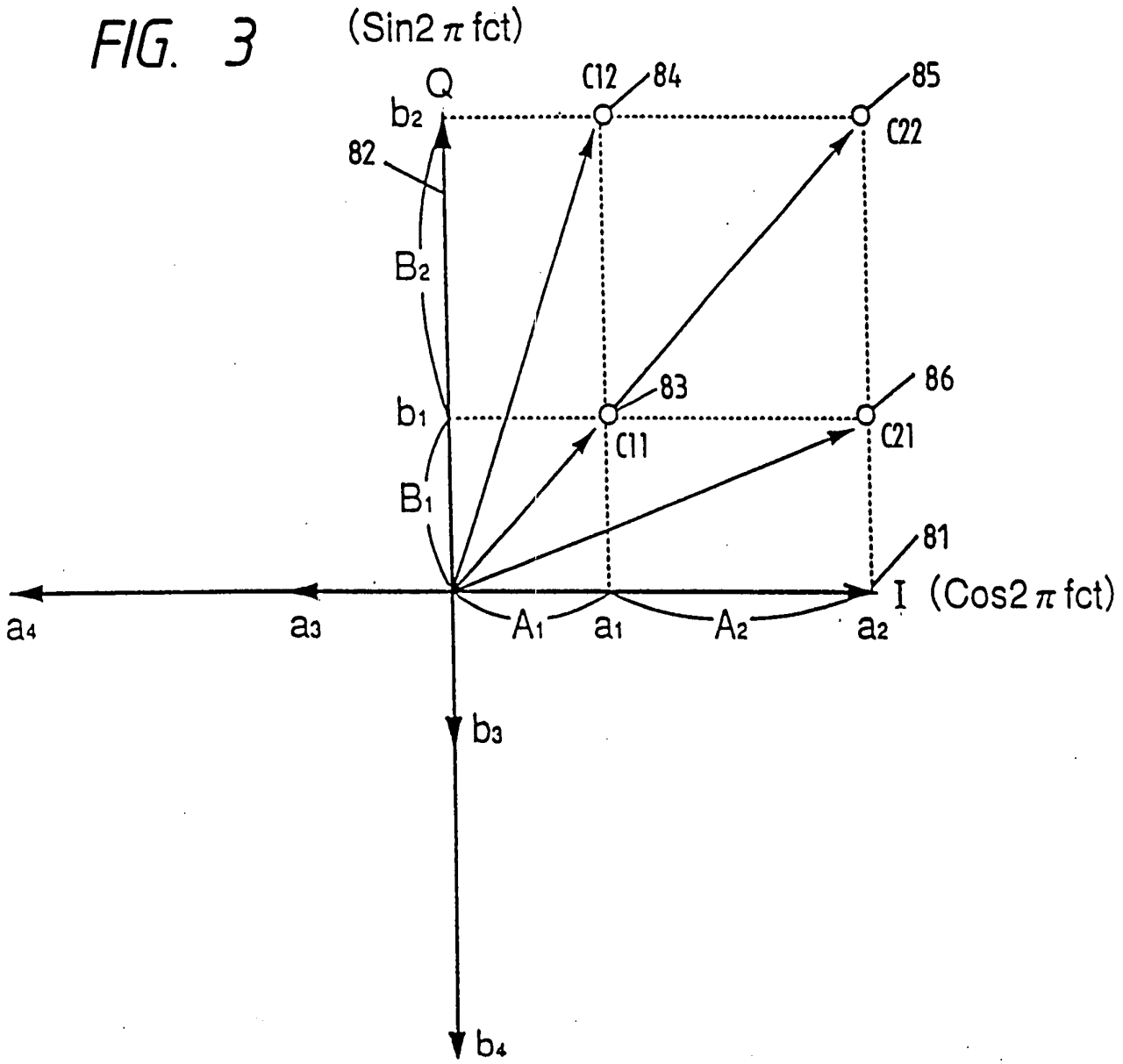

(Sin2 π fct)
Q
C12
84
85
b2
C22
82
B2
83
86
b1
C11
C21
B1
81
I
(Cos2 π fct)
a4
a3
A1
a1
A2
a2
b3
b4

FIG. 4

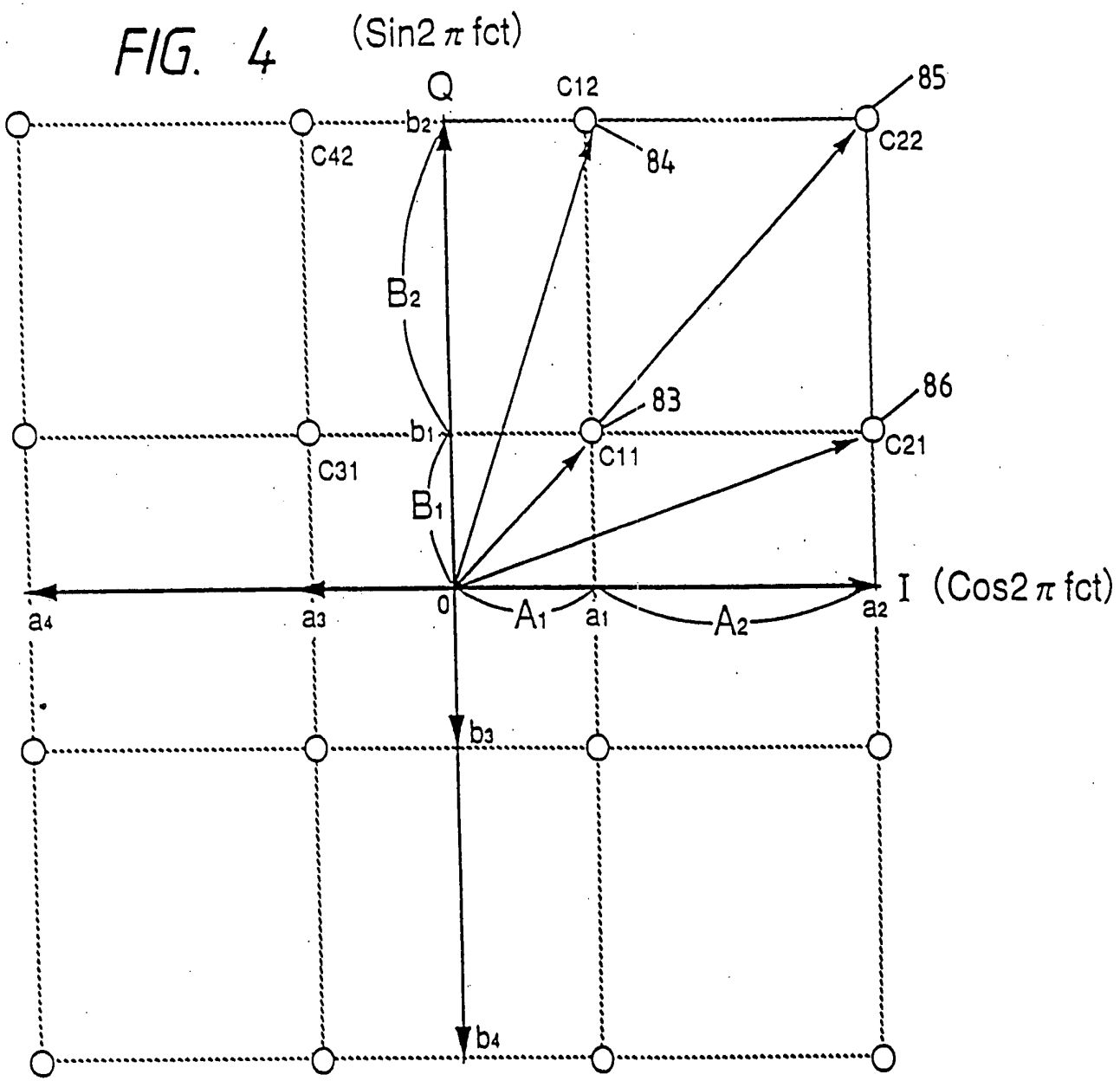

(Sin2 π fct)
Q
C12
85
b2
C42
84
C22
B2
86
83
b1
C21
C31
C11
B1
I (Cos2 π fct)
0
a4
a3
A1
a1
A2
a2
b3
b4

FIG. 5

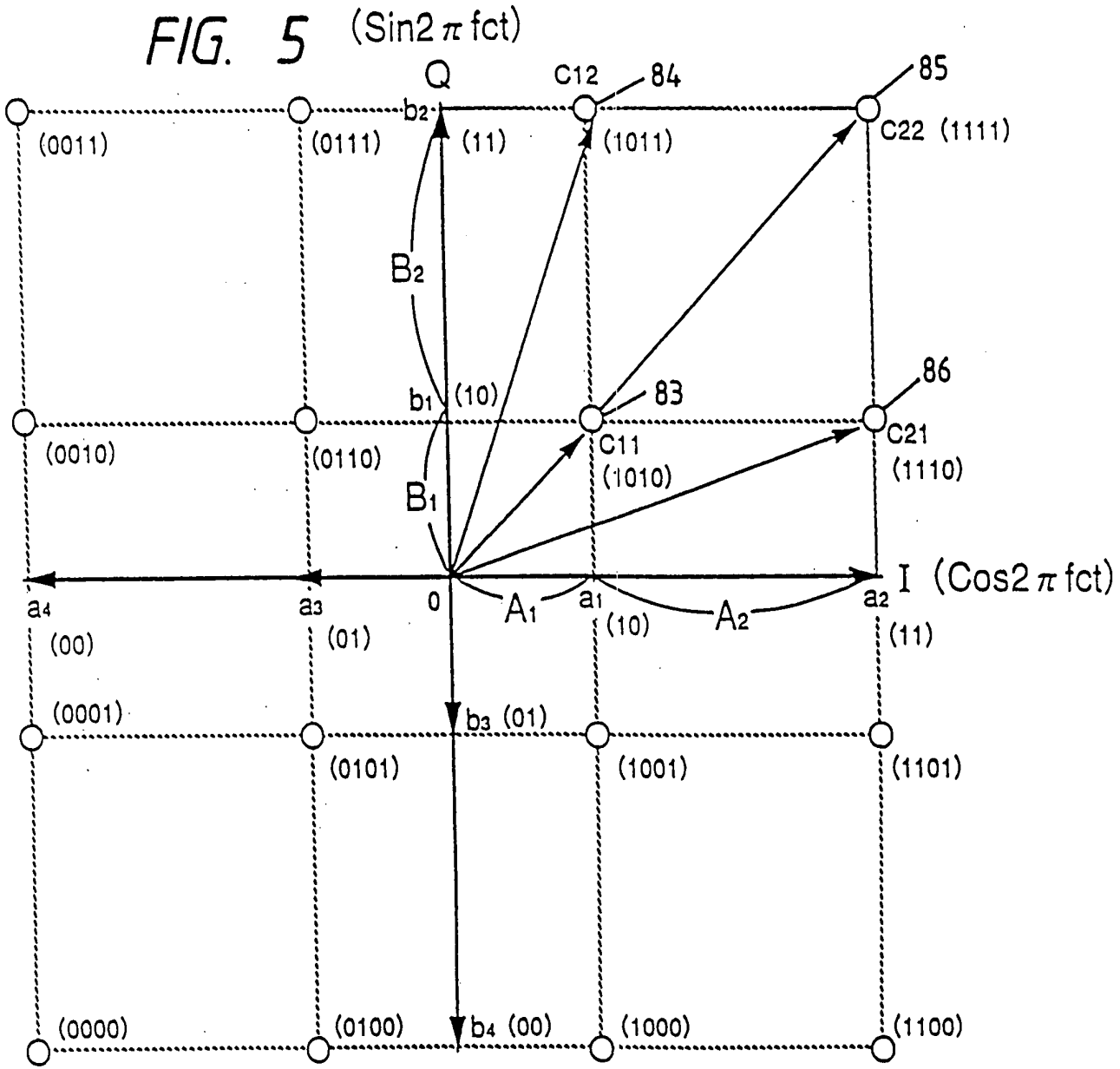

(Sin2 π fct)
Q
C12
84
85
b2
(0011)
(0111)
(11)
(1011)
C22 (1111)
B2
86
b1
(10)
83
(0010)
(0110)
C11
(1010)
C21
(1110)
B1
I (Cos2 π fct)
a4
a3
0
A1
a1
A2
a2
(00)
(01)
(10)
(11)
(0001)
b3 (01)
(0101)
(1001)
(1101)
(0000)
(0100)
b4 (00)
(1000)
(1100)

FIG. 6

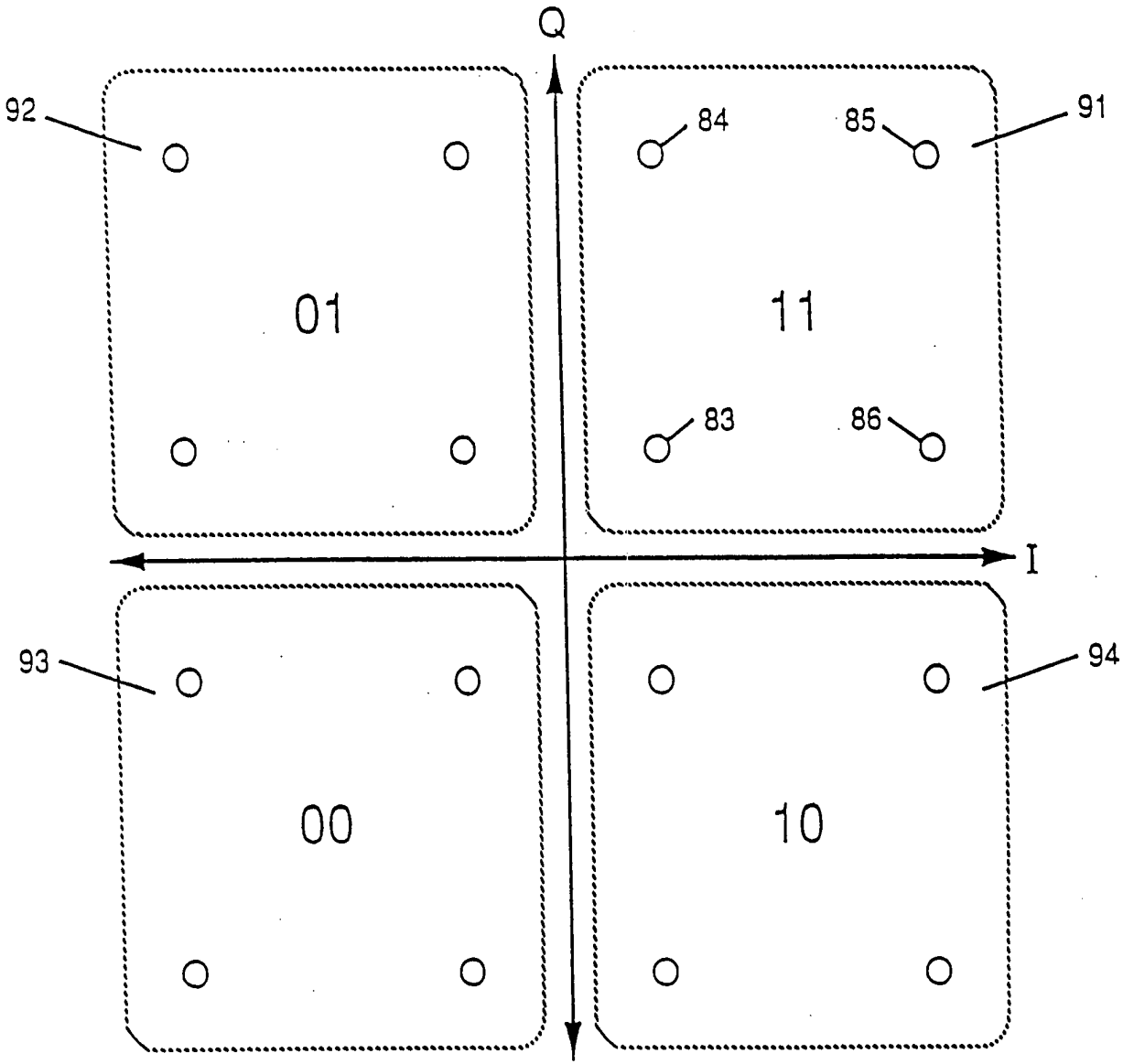


FIG. 7

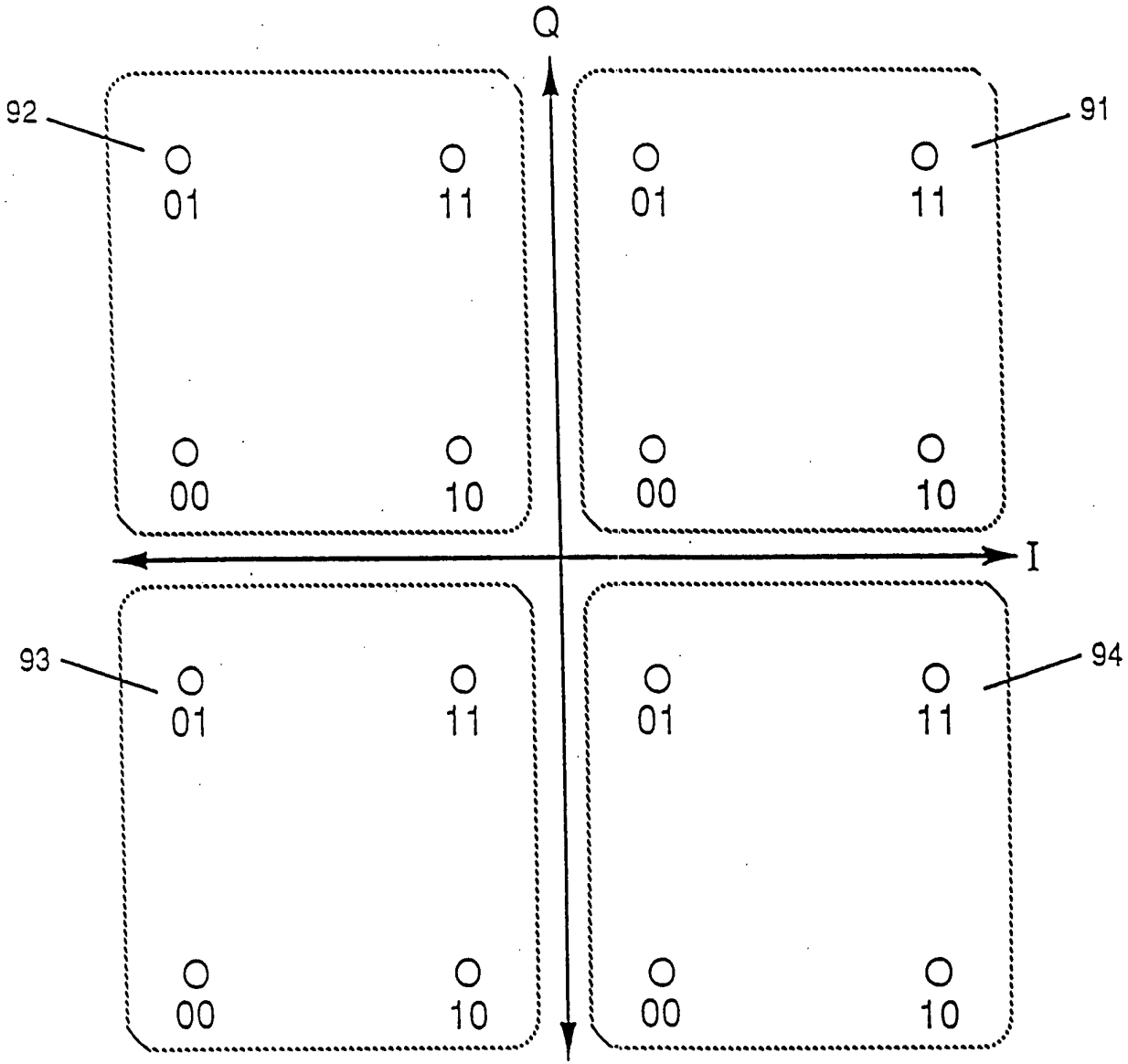


FIG. 8

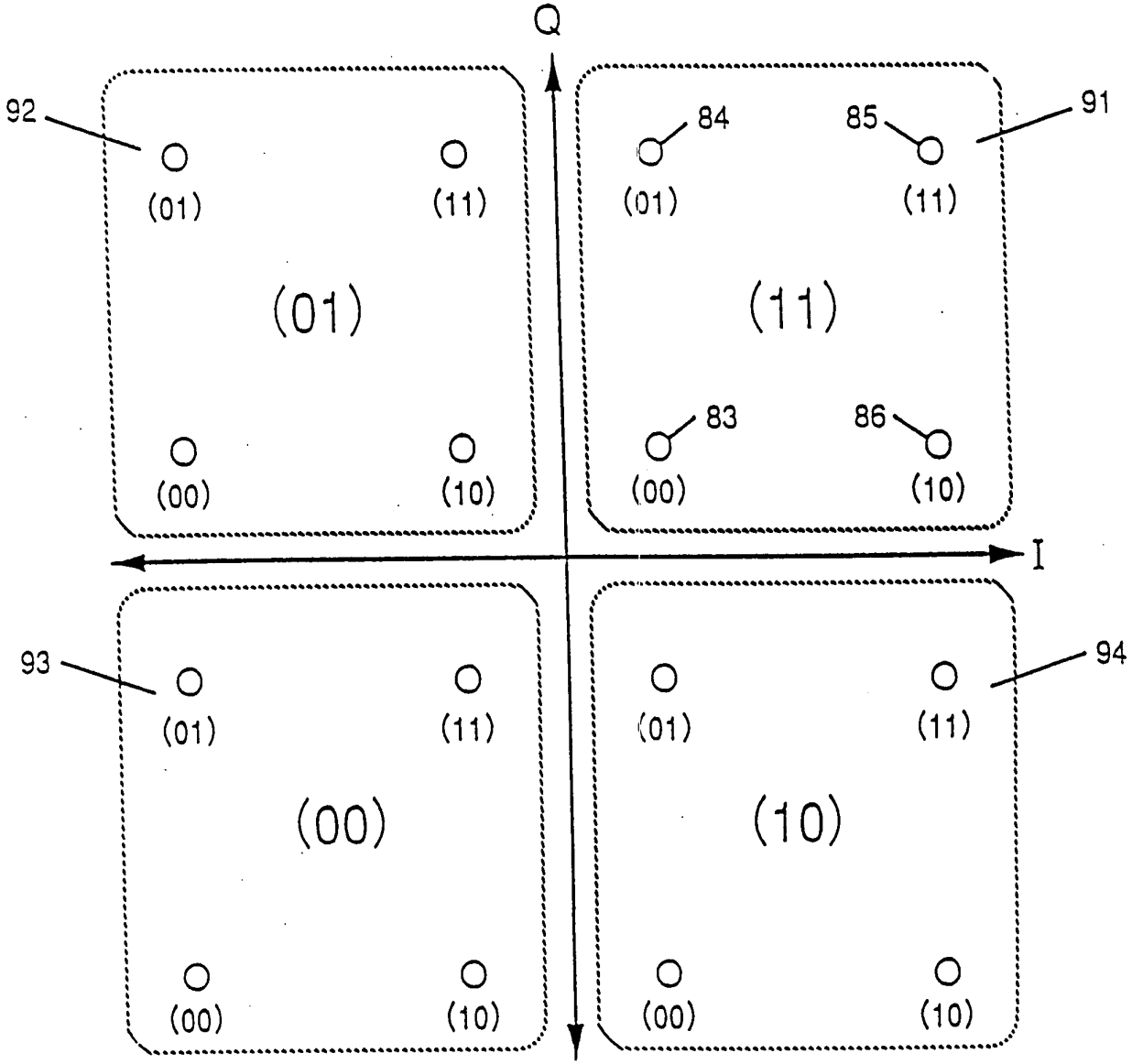

Q
I
92
(01)
(11)
(01)
(00)
(10)
84
85
91
(01)
(11)
(11)
83
86
(00)
(10)
93
(01)
(11)
(00)
(00)
(10)
94
(01)
(11)
(10)
(00)
(10)

FIG. 9

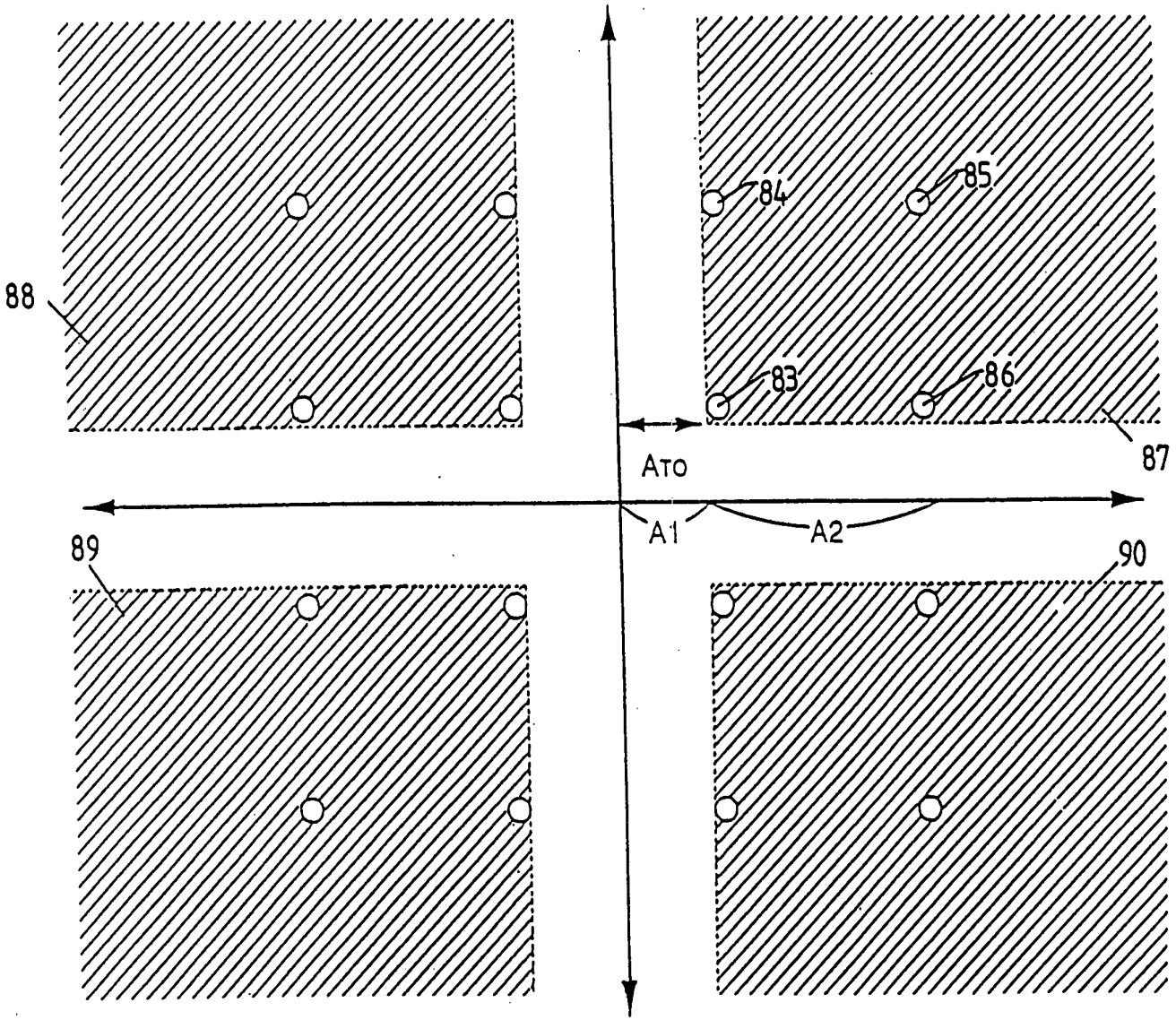


FIG. 10

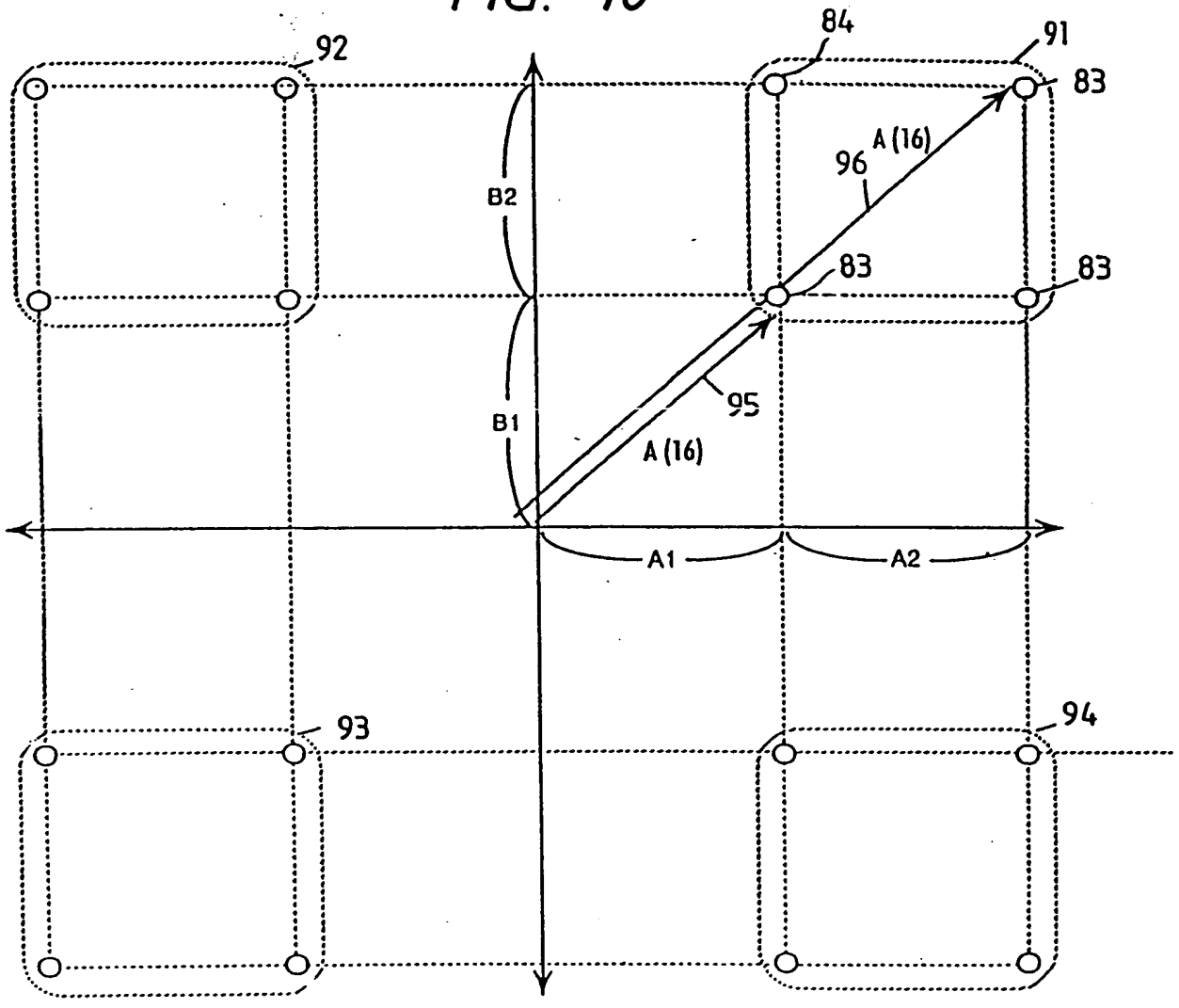


FIG. 11

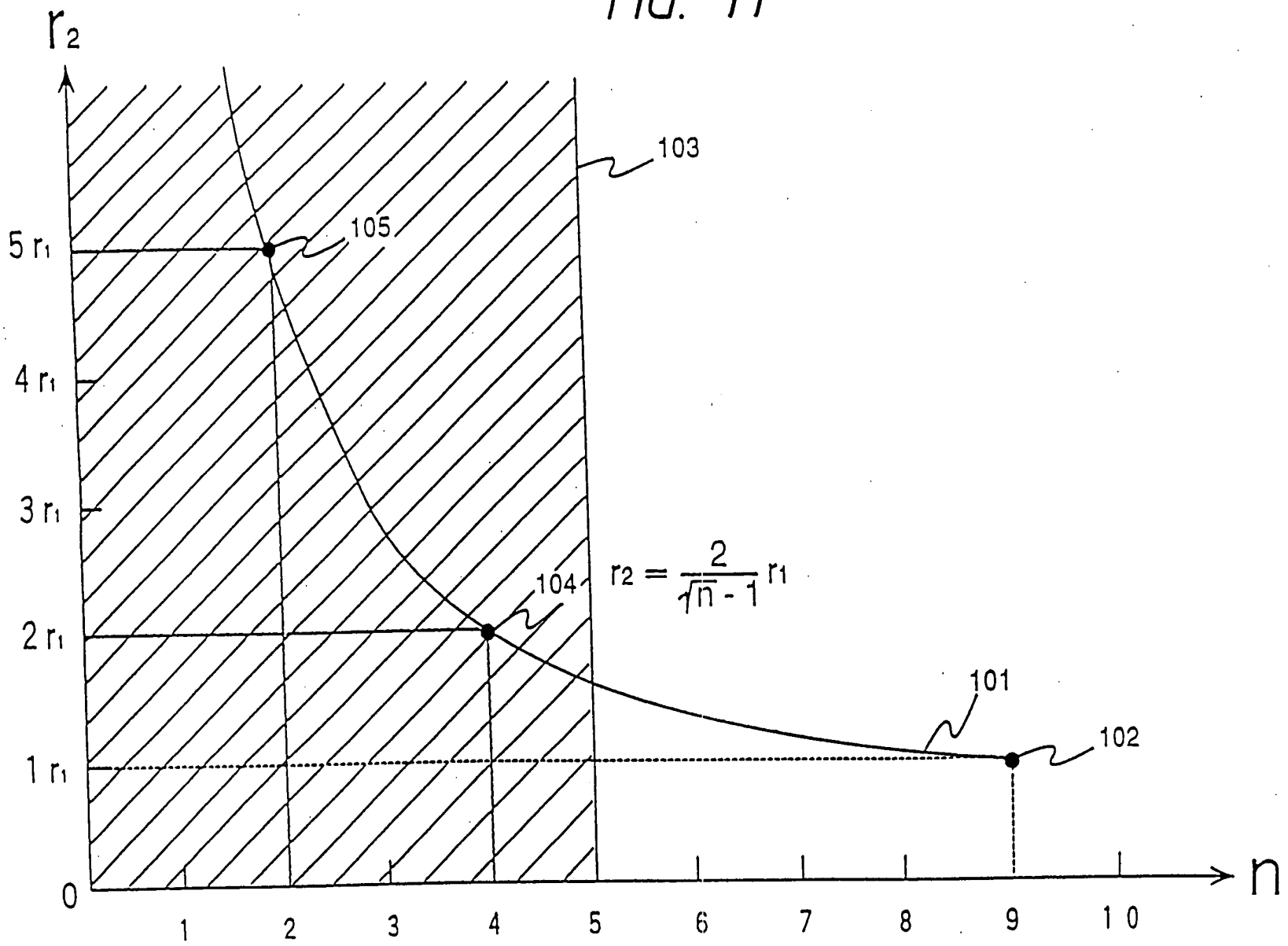

r2
5 r1
4 r1
3 r1
2 r1
1 r1
0
1
2
3
4
5
6
7
8
9
10
n
103
105
104
101
102
r2 = 2/(√n - 1) r1

FIG. 12

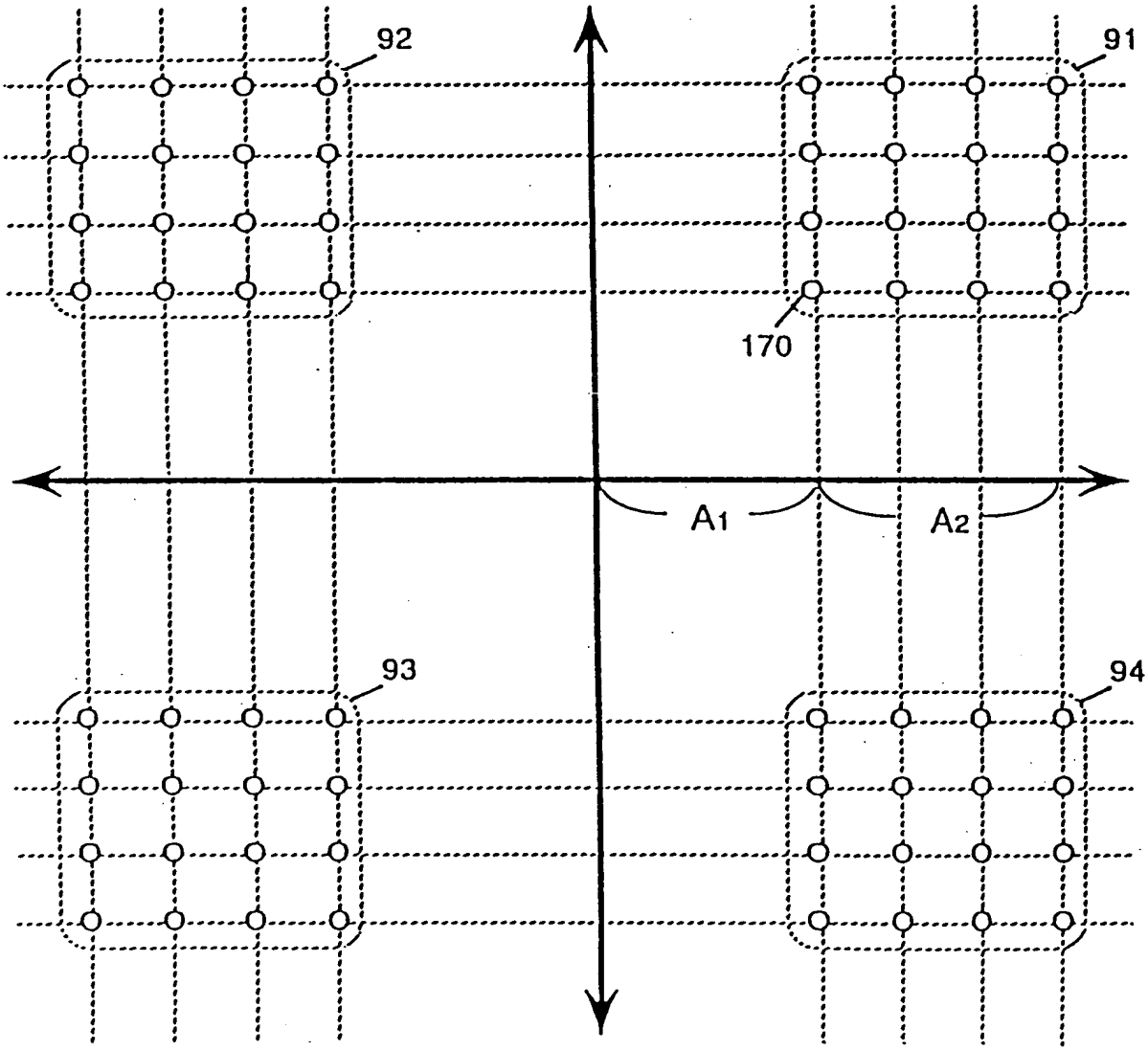


FIG. 13

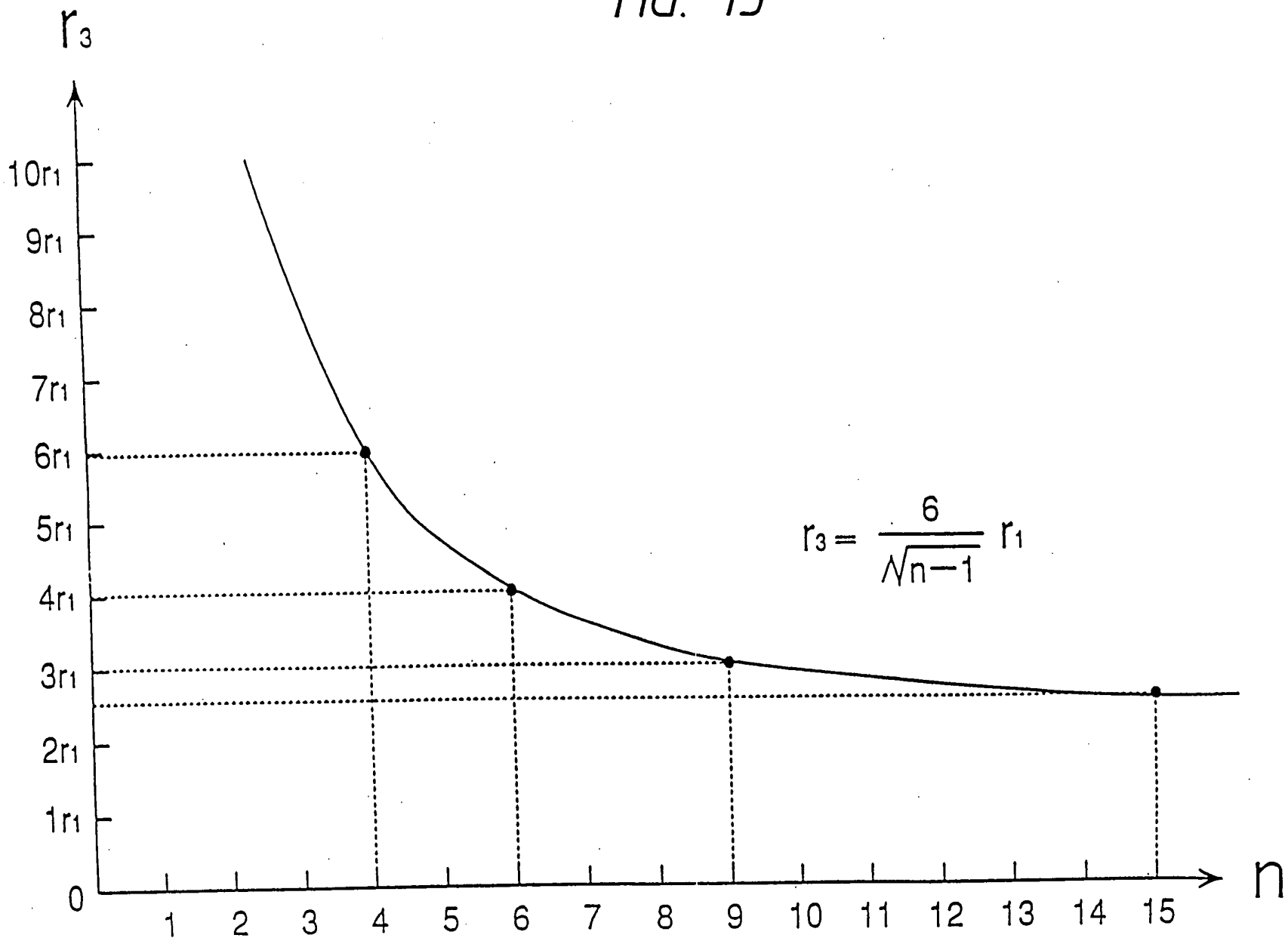

r3
10r1
9r1
8r1
7r1
6r1
5r1
4r1
3r1
2r1
1r1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
n
r3 = 6 / √(n−1) r1

FIG. 14

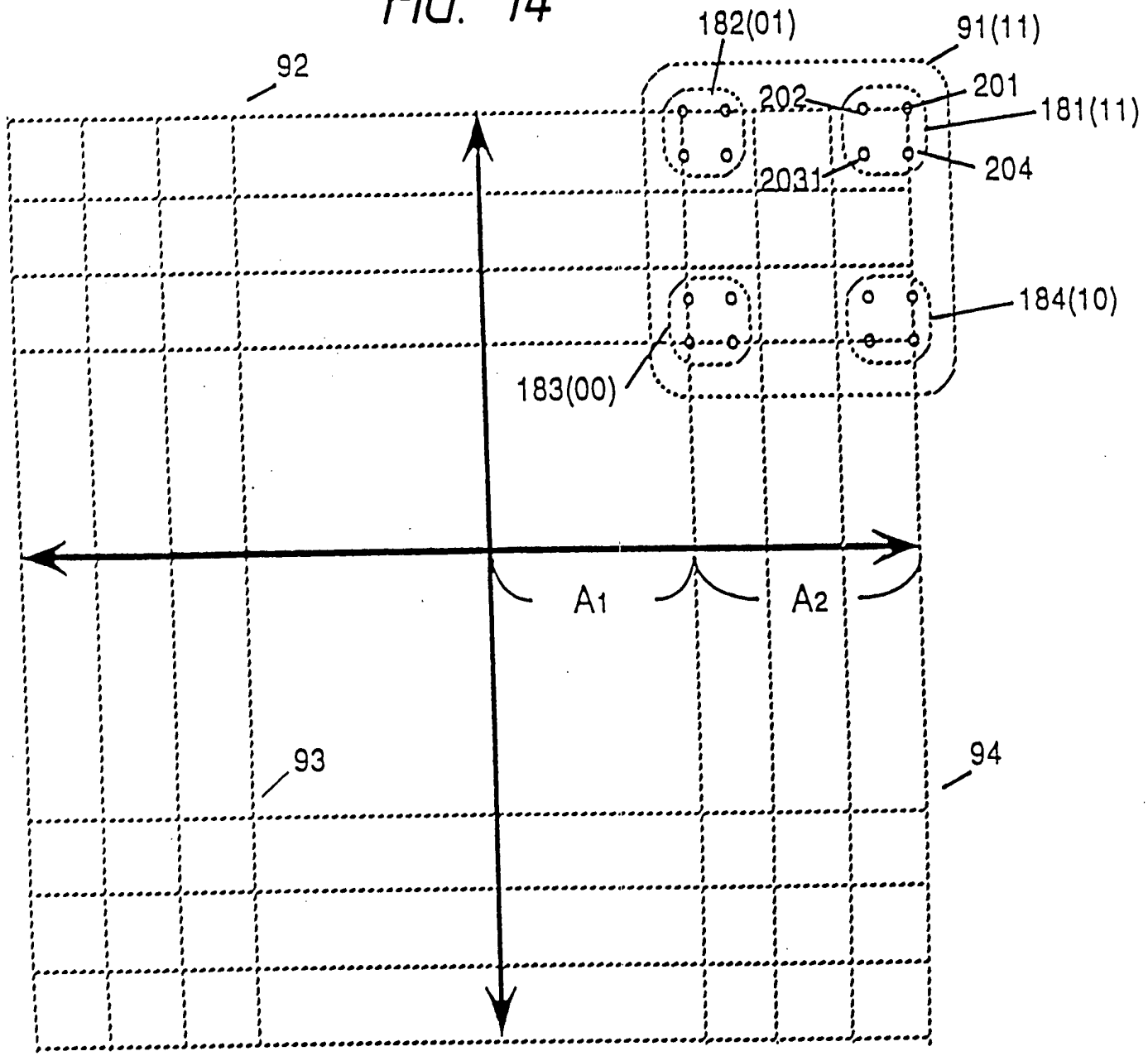


FIG. 15

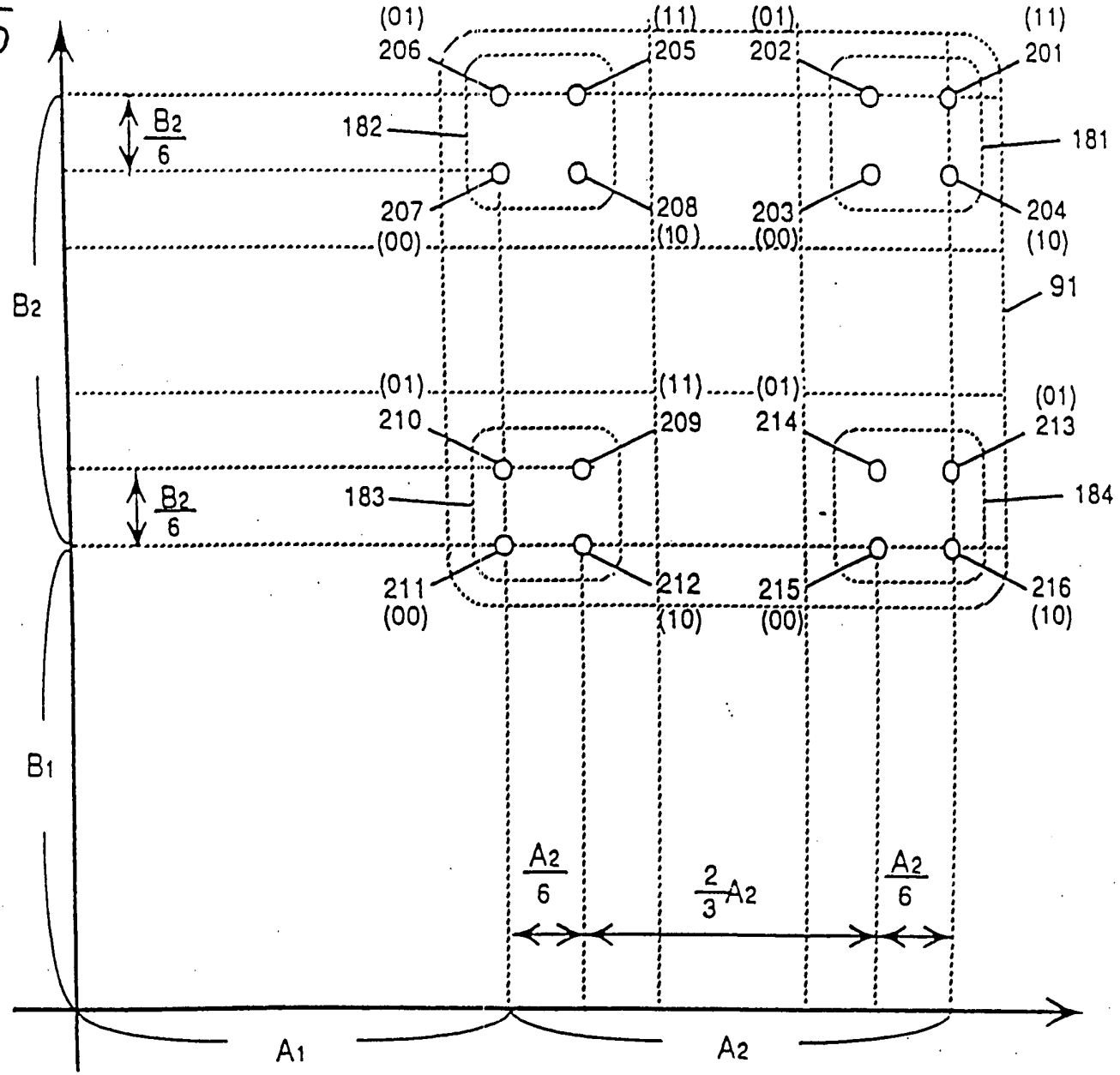

(01)
206
(11)
205
(01)
202
(11)
201
B2/6
182
181
207
208
(10)
203
(00)
204
(10)
(00)
B2
91
(01)
(11)
(01)
(01)
210
209
214
213
B2/6
183
184
211
(00)
212
(10)
215
(00)
216
(10)
B1
A2/6
2/3 A2
A2/6
A1
A2

FIG. 16

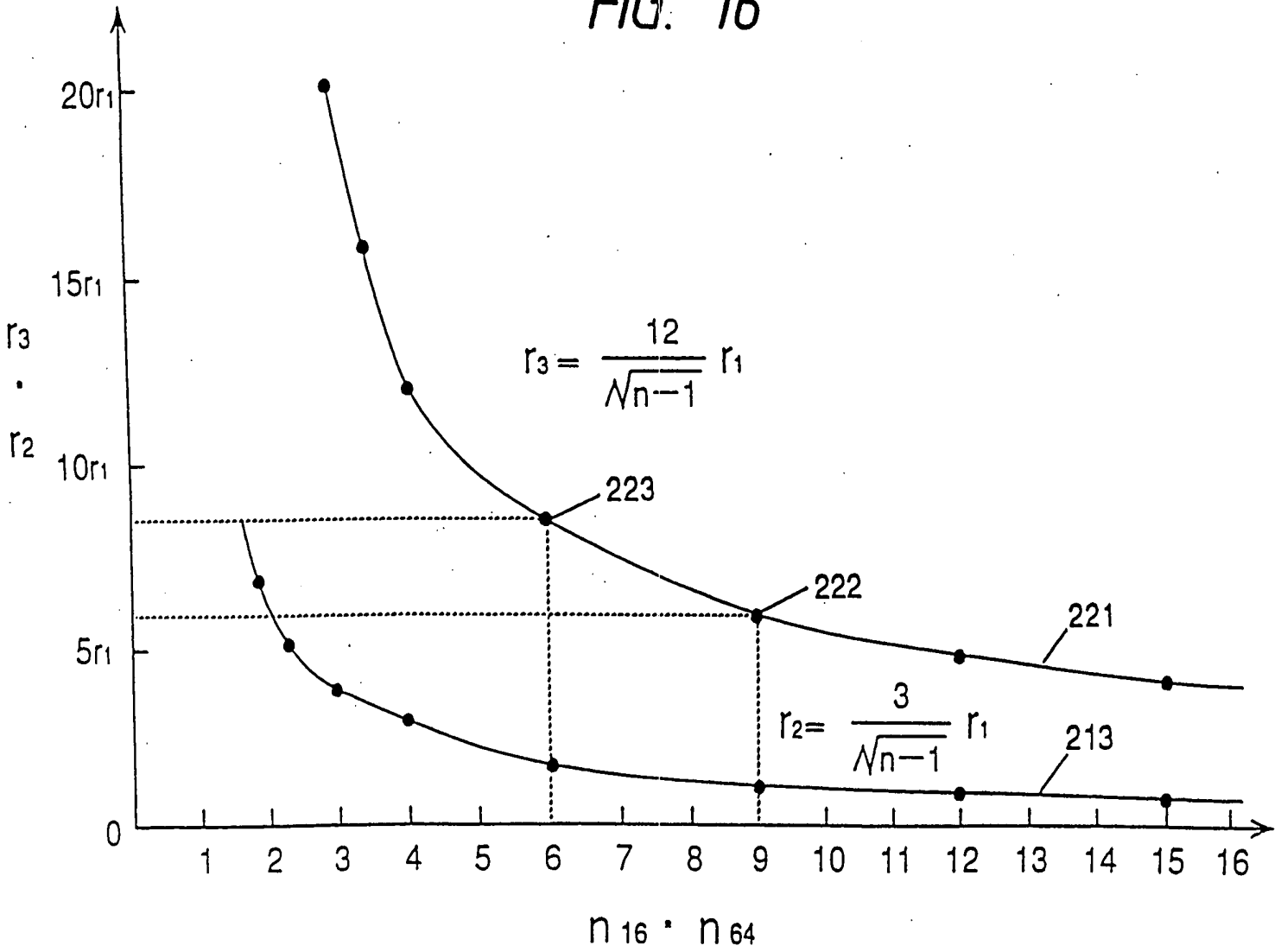

20r1
15r1
10r1
5r1
0
r3
•
r2
$r_3 = \frac{12}{\sqrt{n-1}} r_1$
$r_2 = \frac{3}{\sqrt{n-1}} r_1$
223
222
221
213
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
n 16 • n 64

FIG. 17

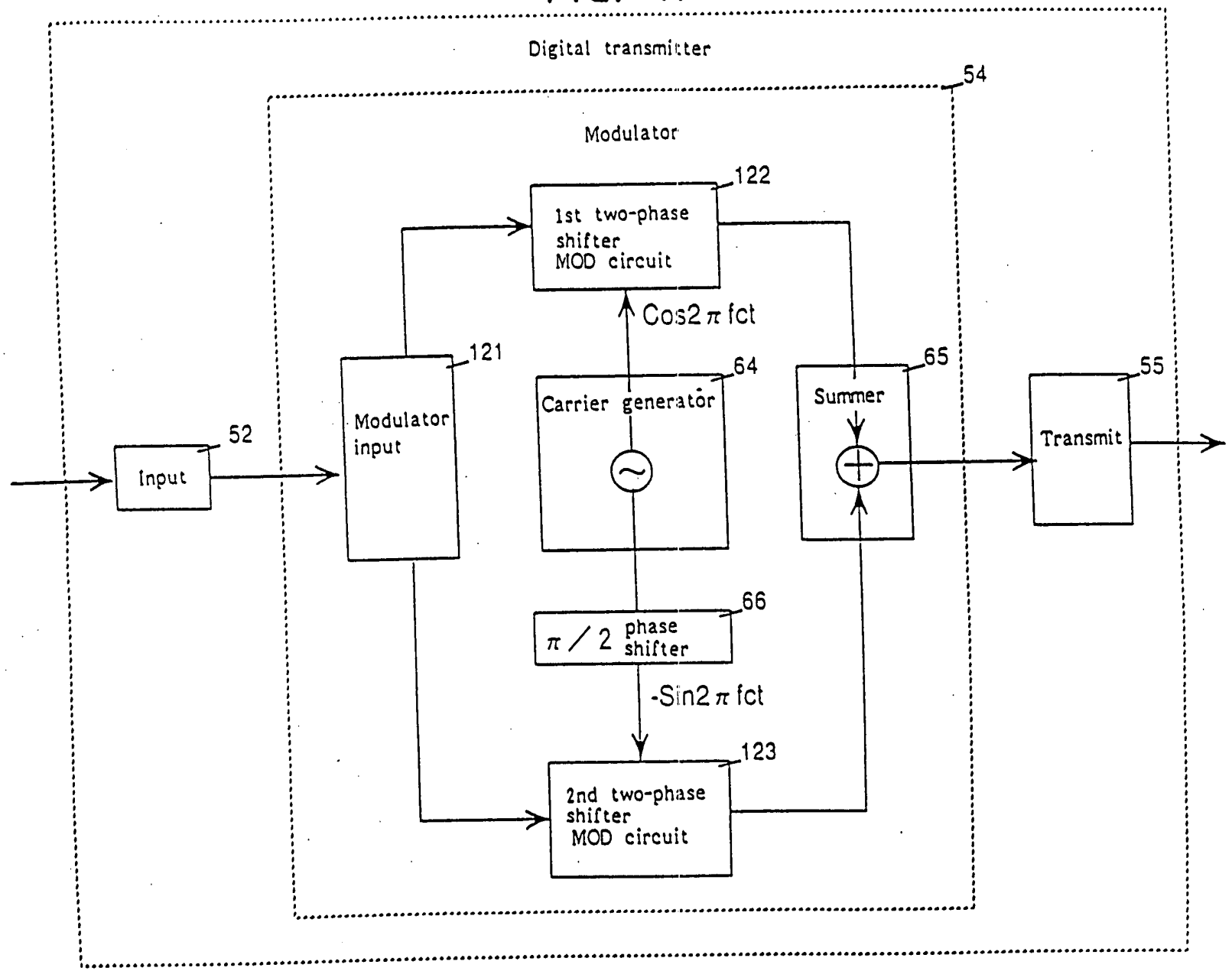

Digital transmitter
54
Modulator
122
1st two-phase shifter MOD circuit
Cos2πfct
121
64
65
55
Modulator input
Carrier generator
Summer
Transmit
52
Input
66
π / 2 phase shifter
-Sin2πfct
123
2nd two-phase shifter MOD circuit

FIG. 18

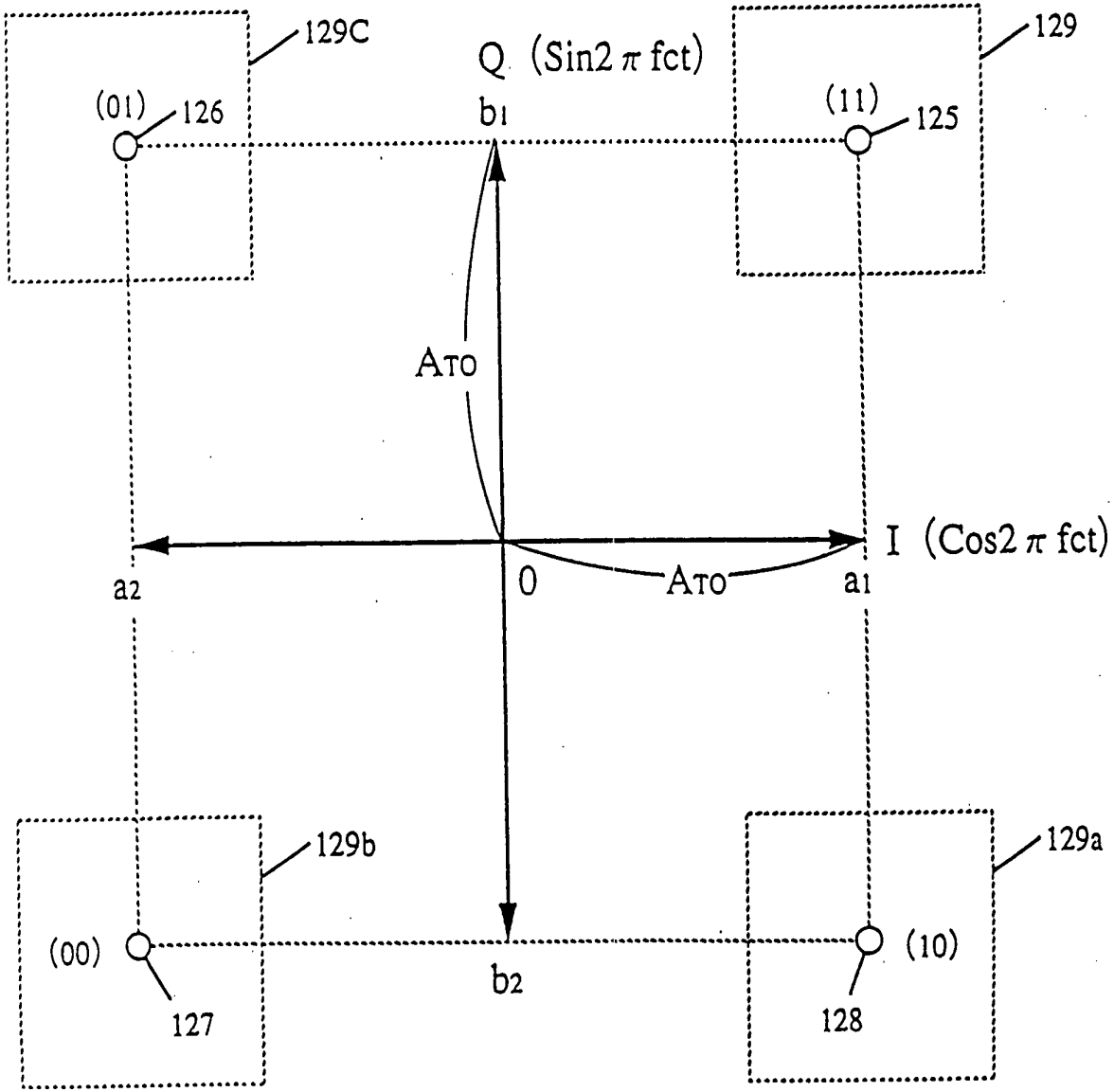

129C
Q (Sin2 π fct)
129
(01)
126
b1
(11)
125
ATO
I (Cos2 π fct)
a2
0
ATO
a1
129b
129a
(00)
127
b2
(10)
128

FIG. 19

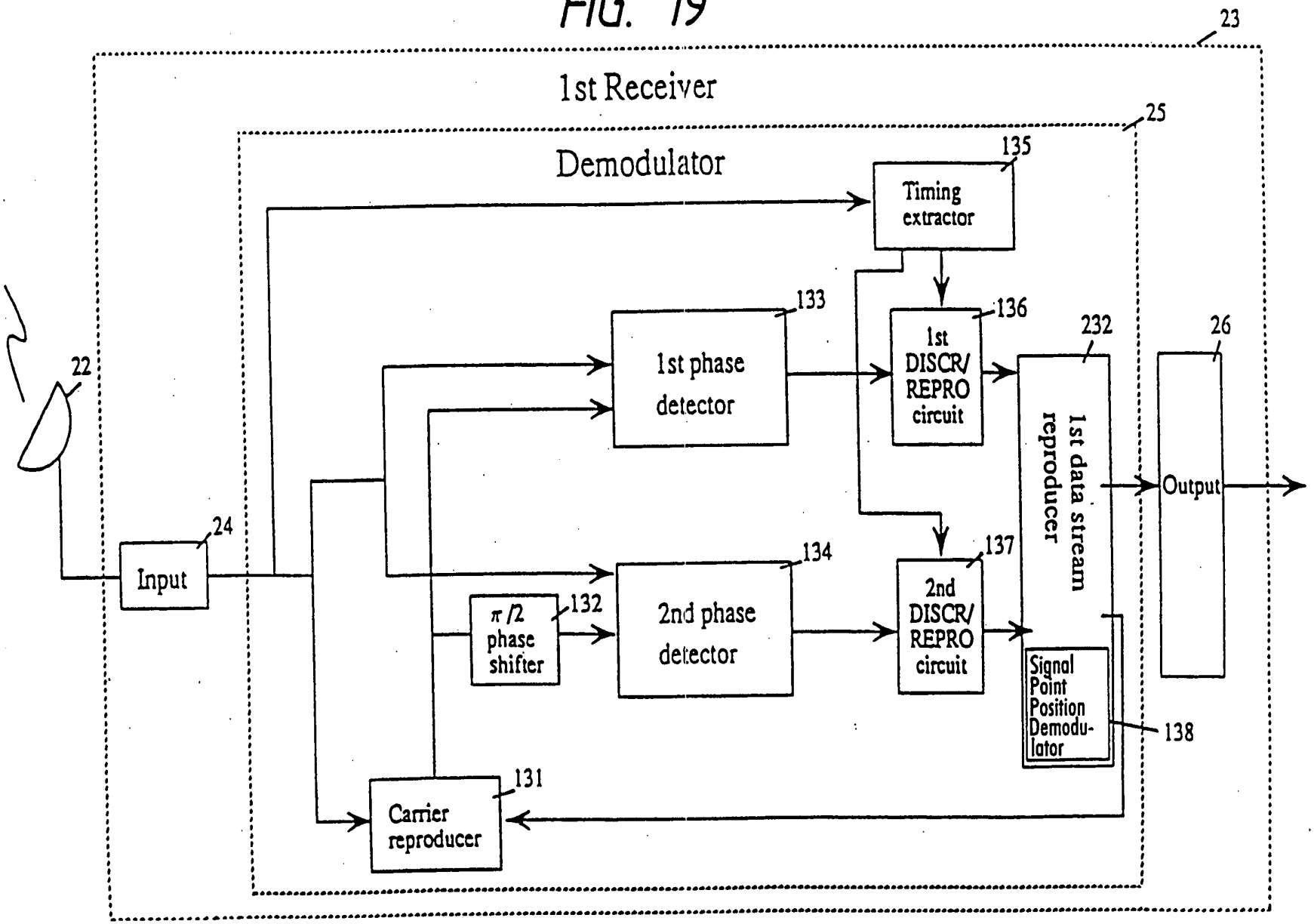

23
1st Receiver
25
Demodulator
135
Timing extractor
133
1st phase detector
136
1st DISCR/ REPRO circuit
232
1st data stream reproducer
26
Output
22
24
Input
134
2nd phase detector
137
2nd DISCR/ REPRO circuit
π/2 phase shifter
132
Signal Point Position Demodu-lator
138
131
Carrier reproducer

FIG. 20

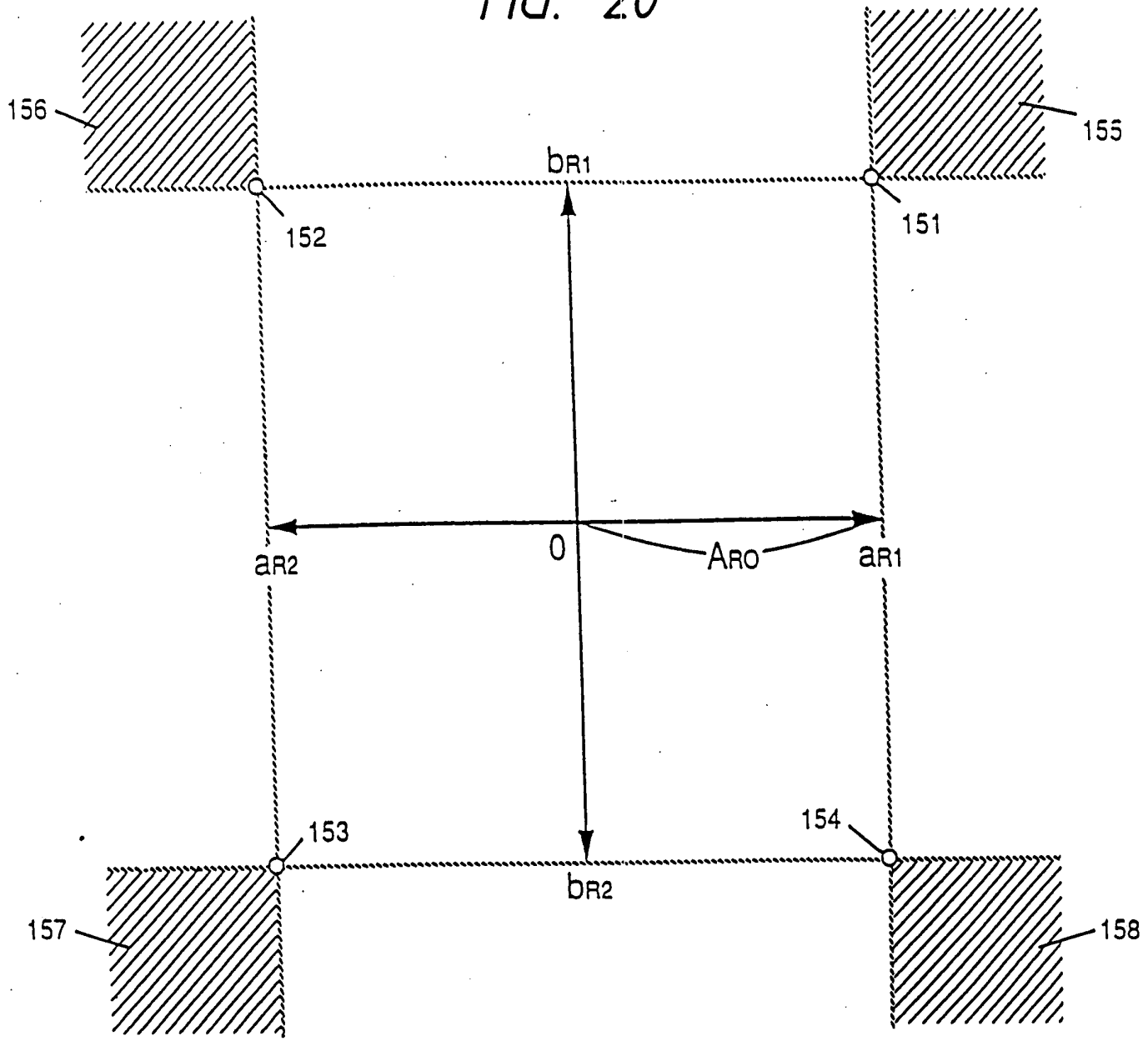


FIG. 21

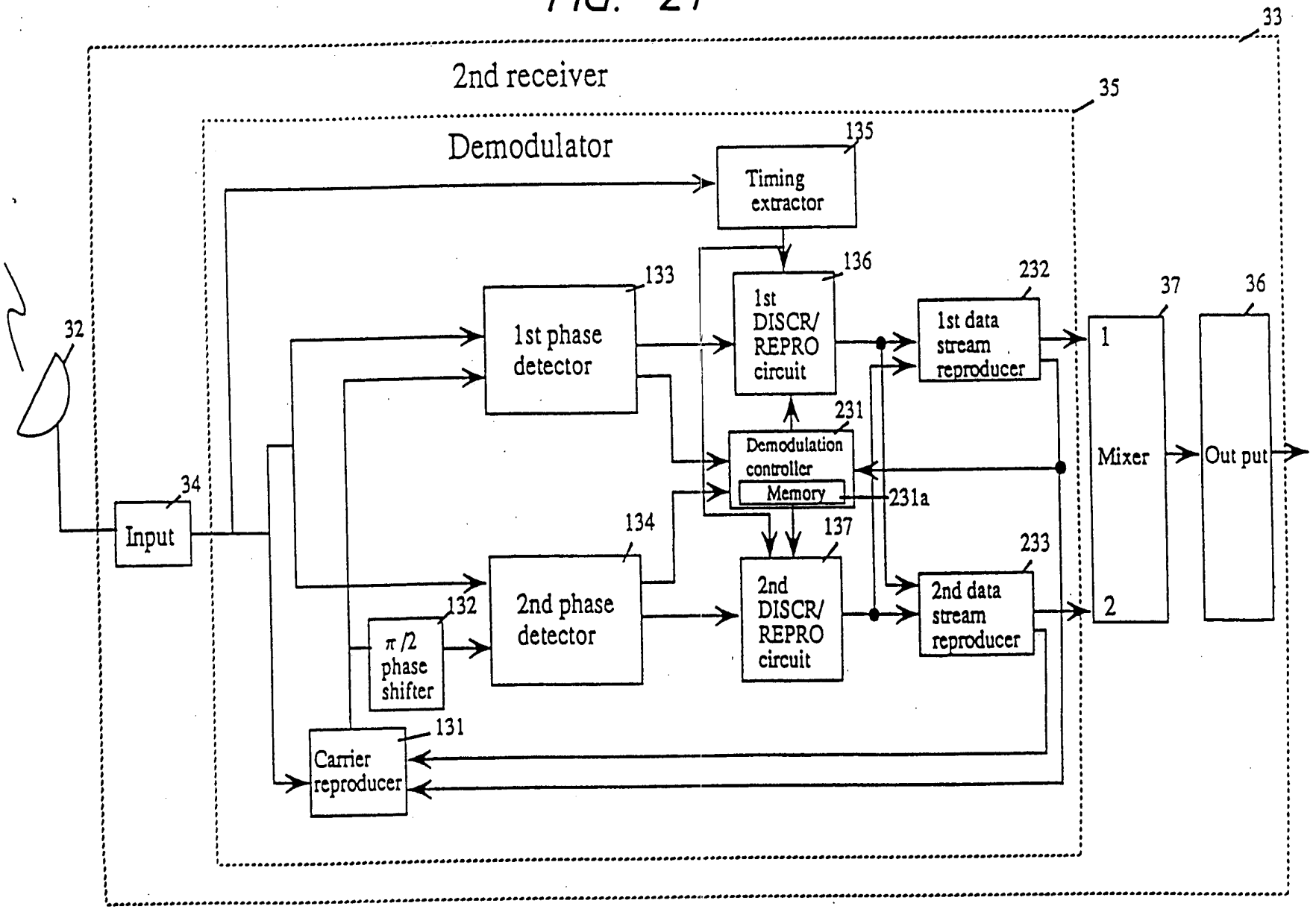

33
2nd receiver
35
Demodulator
135
Timing extractor
136
1st DISCR/ REPRO circuit
133
1st phase detector
232
1st data stream reproducer
37
36
32
231
Demodulation controller
Memory
231a
Mixer
Out put
34
Input
134
137
233
2nd phase detector
2nd DISCR/ REPRO circuit
2nd data stream reproducer
132
π /2 phase shifter
131
Carrier reproducer

FIG. 22

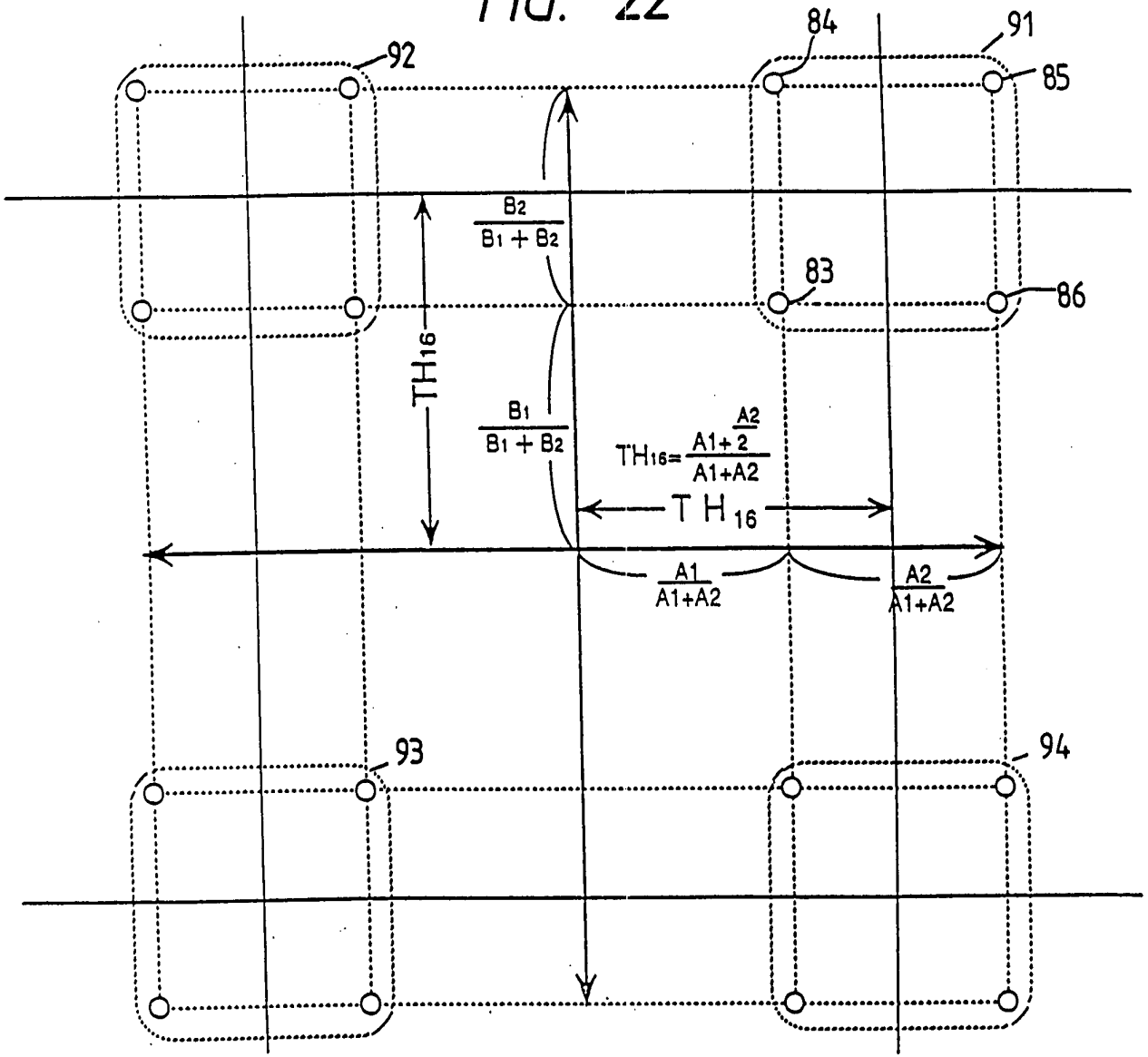

92
84
91
85
83
86
93
94
TH_{16}
$\frac{B_2}{B_1+B_2}$
$\frac{B_1}{B_1+B_2}$
$TH_{16}=\frac{A1+\frac{A2}{2}}{A1+A2}$
TH_{16}
$\frac{A1}{A1+A2}$
$\frac{A2}{A1+A2}$

FIG. 23

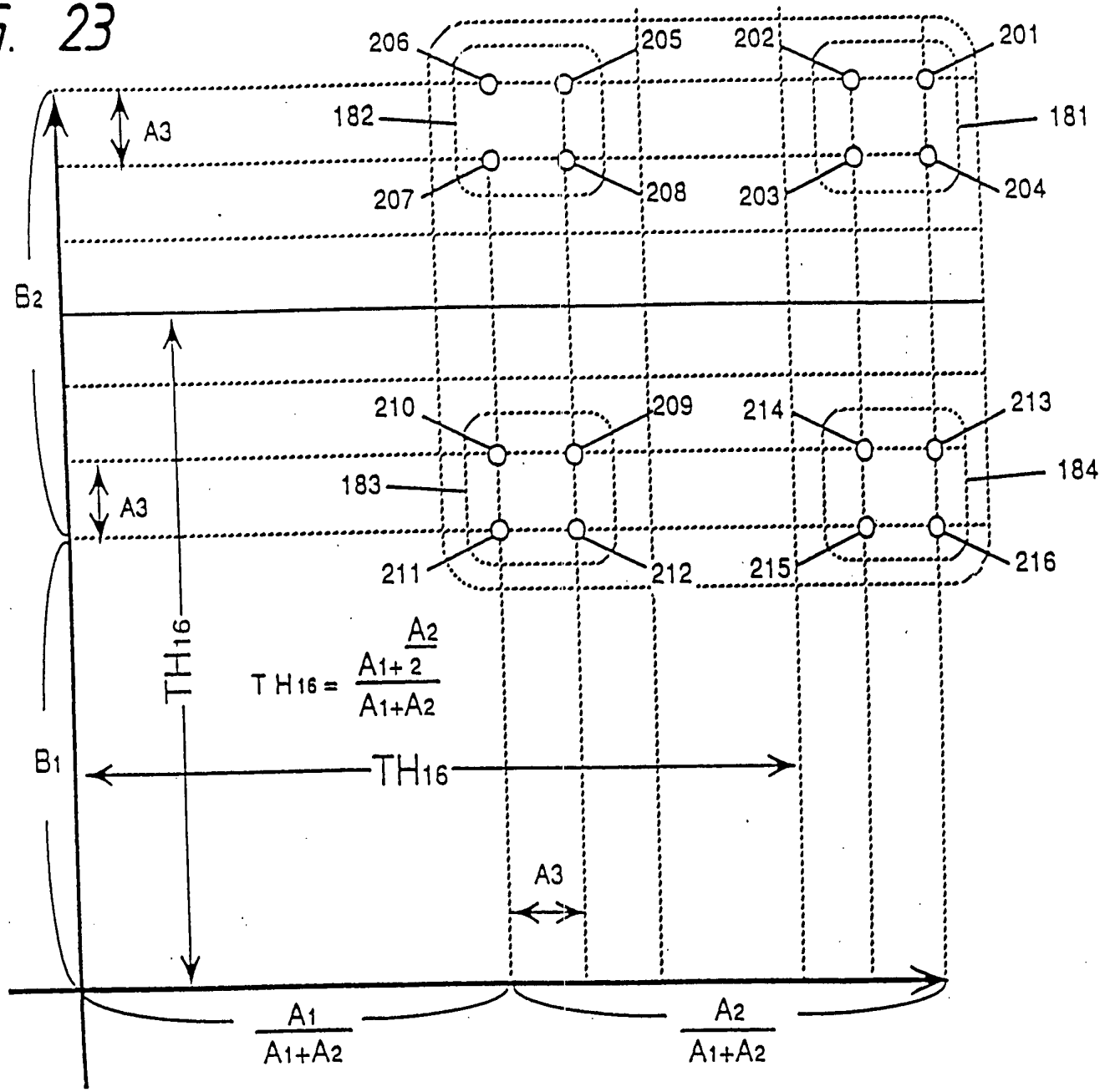

206
205
202
201
182
181
A3
207
208
203
204
B2
210
209
214
213
183
184
A3
211
212
215
216
TH16
TH16 = A2 / (A1+2 / A1+A2)
B1
TH16
A3
A1 / A1+A2
A2 / A1+A2

FIG. 24

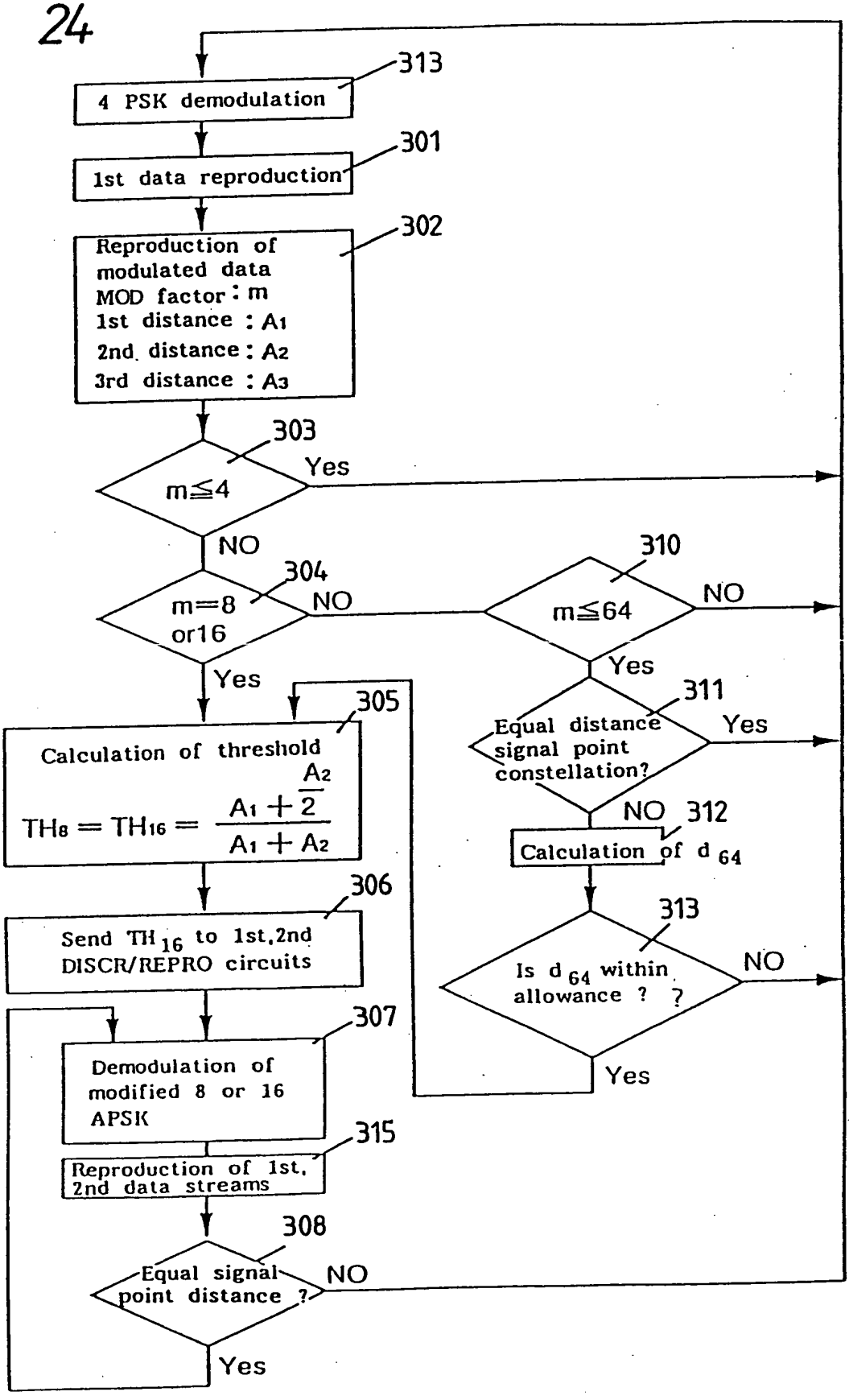

313
4 PSK demodulation
301
1st data reproduction
302
Reproduction of modulated data
MOD factor : m
1st distance : A1
2nd distance : A2
3rd distance : A3
303
m≦4
Yes
NO
304
m=8 or16
NO
Yes
310
m≦64
NO
Yes
311
Equal distance signal point constellation?
Yes
NO
312
Calculation of d 64
313
Is d 64 within allowance ? ?
NO
Yes
305
Calculation of threshold
TH8 = TH16 = (A1 + A2/2) / (A1 + A2)
306
Send TH 16 to 1st,2nd DISCR/REPRO circuits
307
Demodulation of modified 8 or 16 APSK
315
Reproduction of 1st, 2nd data streams
308
Equal signal point distance ?
NO
Yes

FIG. 25(a)

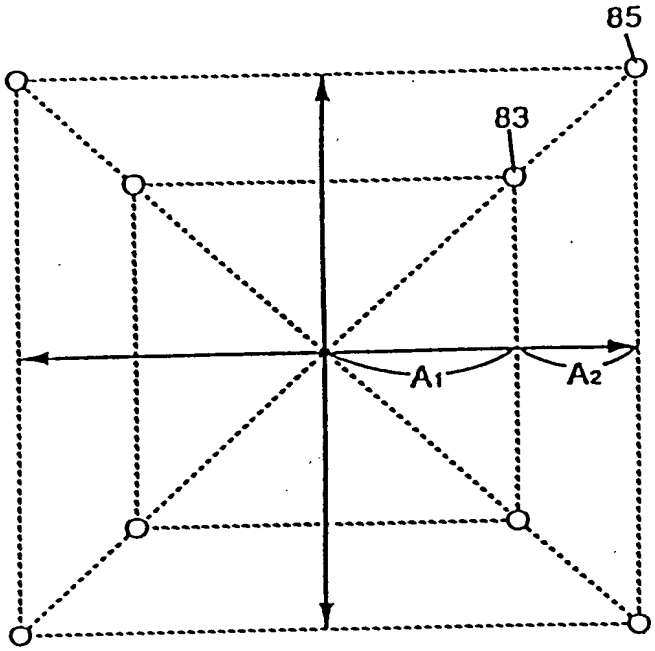


FIG. 25(b)

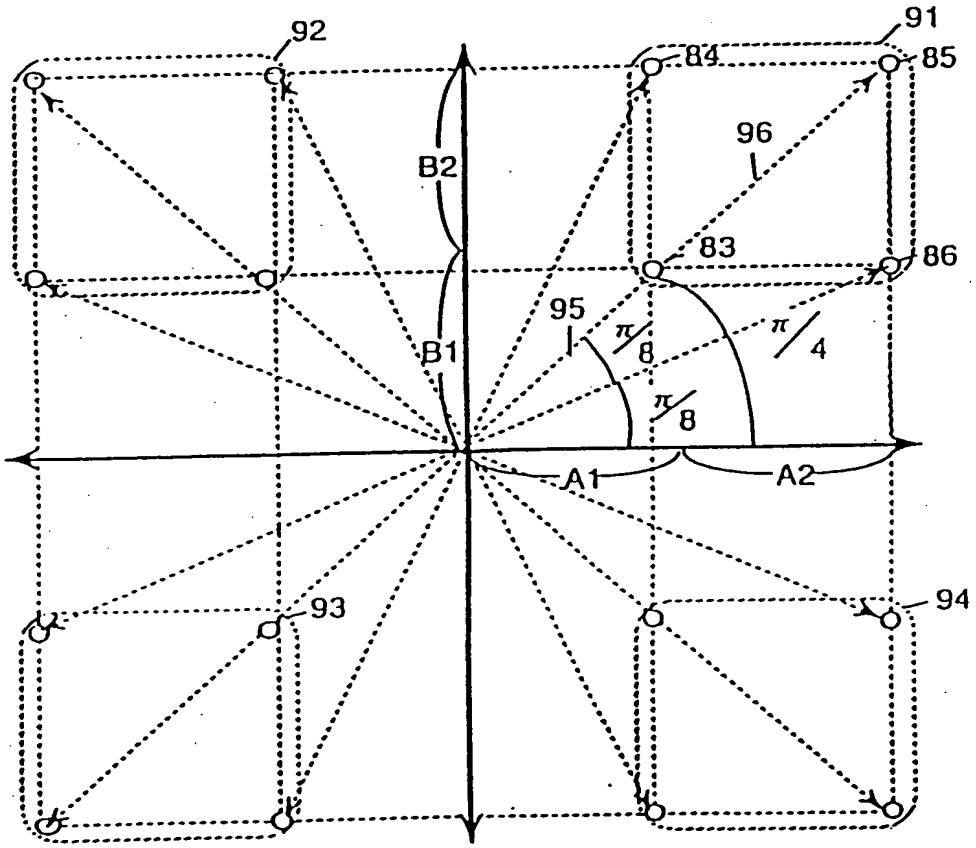


FIG. 26

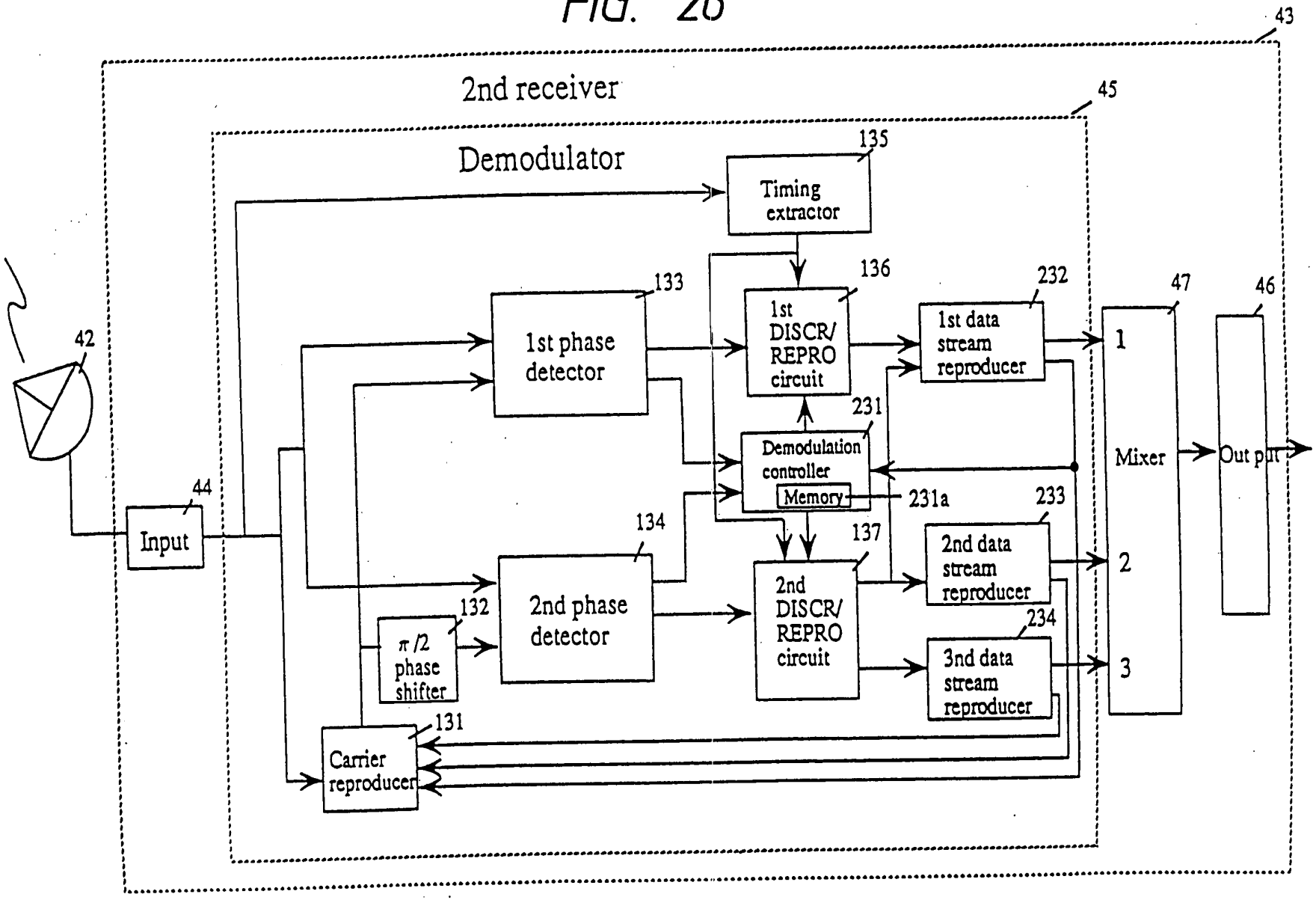

43
2nd receiver
45
Demodulator
135
Timing extractor
136
133
1st phase detector
1st DISCR/ REPRO circuit
232
1st data stream reproducer
47
46
42
231
Demodulation controller
Memory
231a
Mixer
Out put
44
Input
134
137
233
2nd data stream reproducer
2nd phase detector
2nd DISCR/ REPRO circuit
132
π/2 phase shifter
234
3nd data stream reproducer
131
Carrier reproducer
1
2
3

FIG. 27

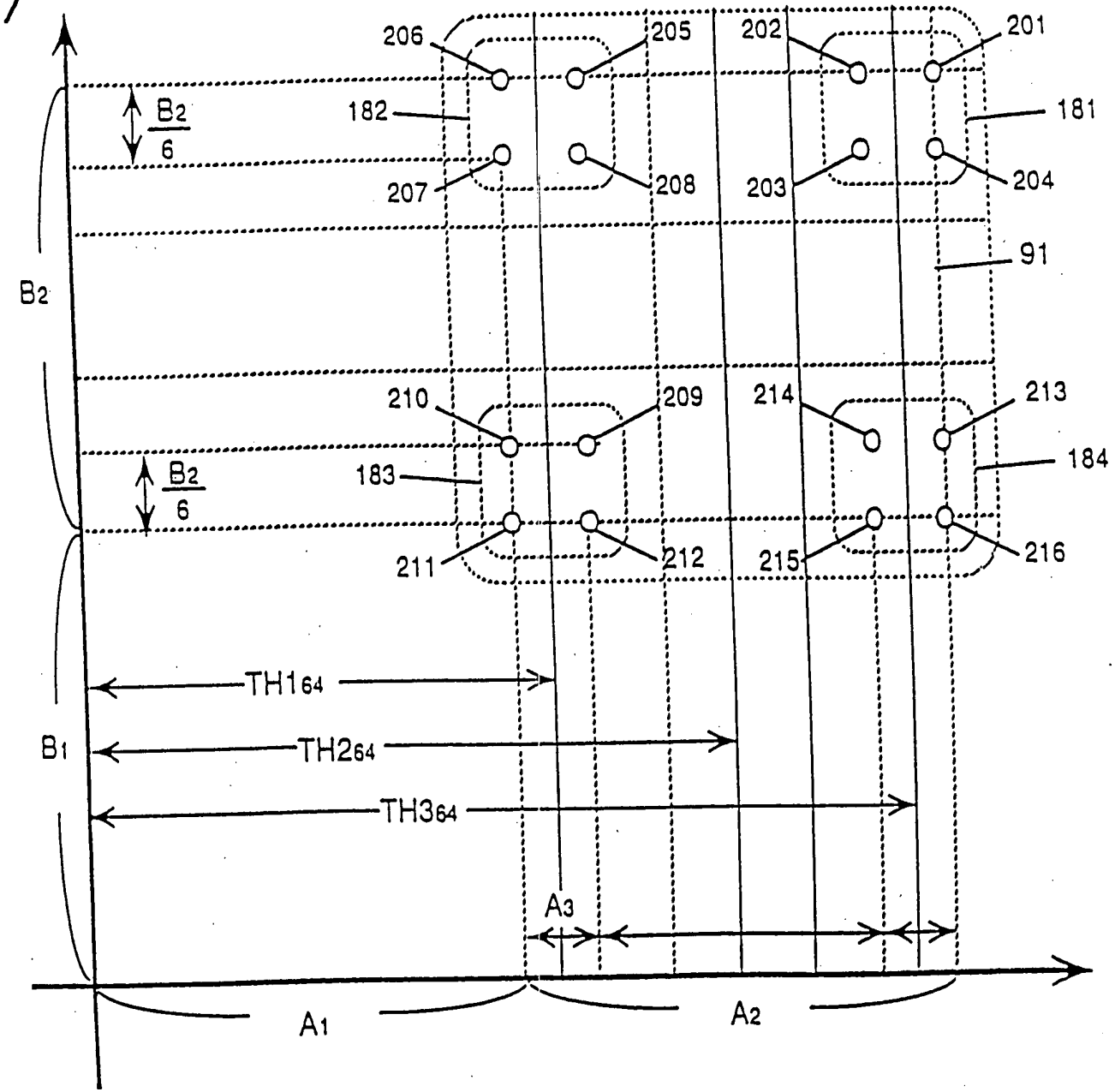

206
205
202
201
182
181
207
208
203
204
91
210
209
214
213
183
184
211
212
215
216
B2
B2/6
B2/6
B1
TH164
TH264
TH364
A3
A1
A2

FIG. 28

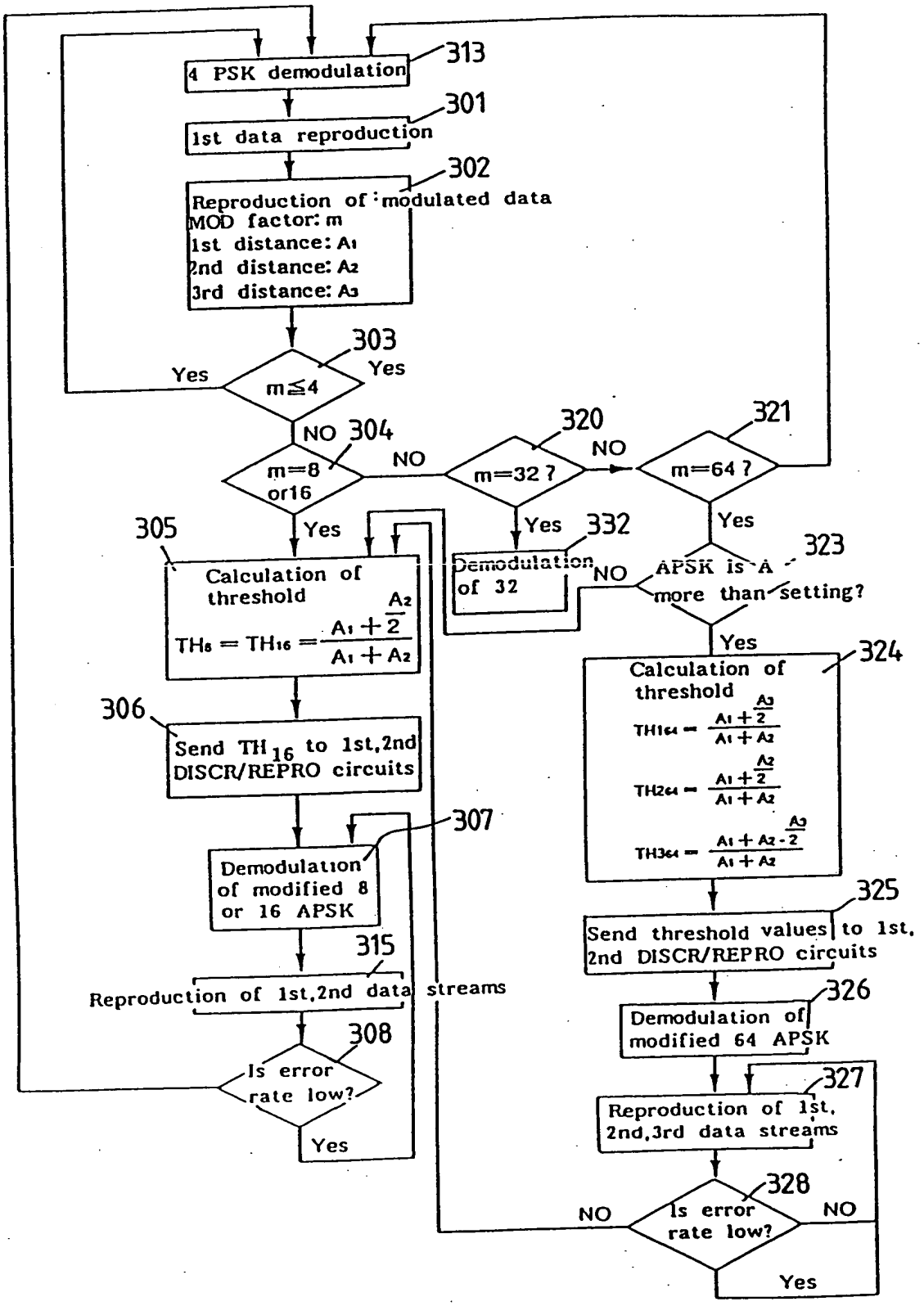

4 PSK demodulation
313
1st data reproduction
301
Reproduction of modulated data
MOD factor: m
1st distance: A1
2nd distance: A2
3rd distance: A3
302
m≦4
303
Yes
NO
m=8 or16
304
NO
m=32 ?
320
NO
m=64 ?
321
Yes
Yes
Yes
305
Calculation of threshold
$TH_8 = TH_{16} = \frac{A_1 + \frac{A_2}{2}}{A_1 + A_2}$
306
Send TH_{16} to 1st,2nd DISCR/REPRO circuits
307
Demodulation of modified 8 or 16 APSK
315
Reproduction of 1st,2nd data streams
308
Is error rate low?
Yes
Demodulation of 32
332
NO
APSK is A more than setting?
323
Yes
Calculation of threshold
324
$TH_{16} = \frac{A_1 + \frac{A_3}{2}}{A_1 + A_2}$
$TH_{26} = \frac{A_1 + \frac{A_2}{2}}{A_1 + A_2}$
$TH_{36} = \frac{A_1 + A_2 - \frac{A_3}{2}}{A_1 + A_2}$
Send threshold values to 1st, 2nd DISCR/REPRO circuits
325
Demodulation of modified 64 APSK
326
Reproduction of 1st, 2nd,3rd data streams
327
Is error rate low?
328
NO
NO
Yes

FIG. 29

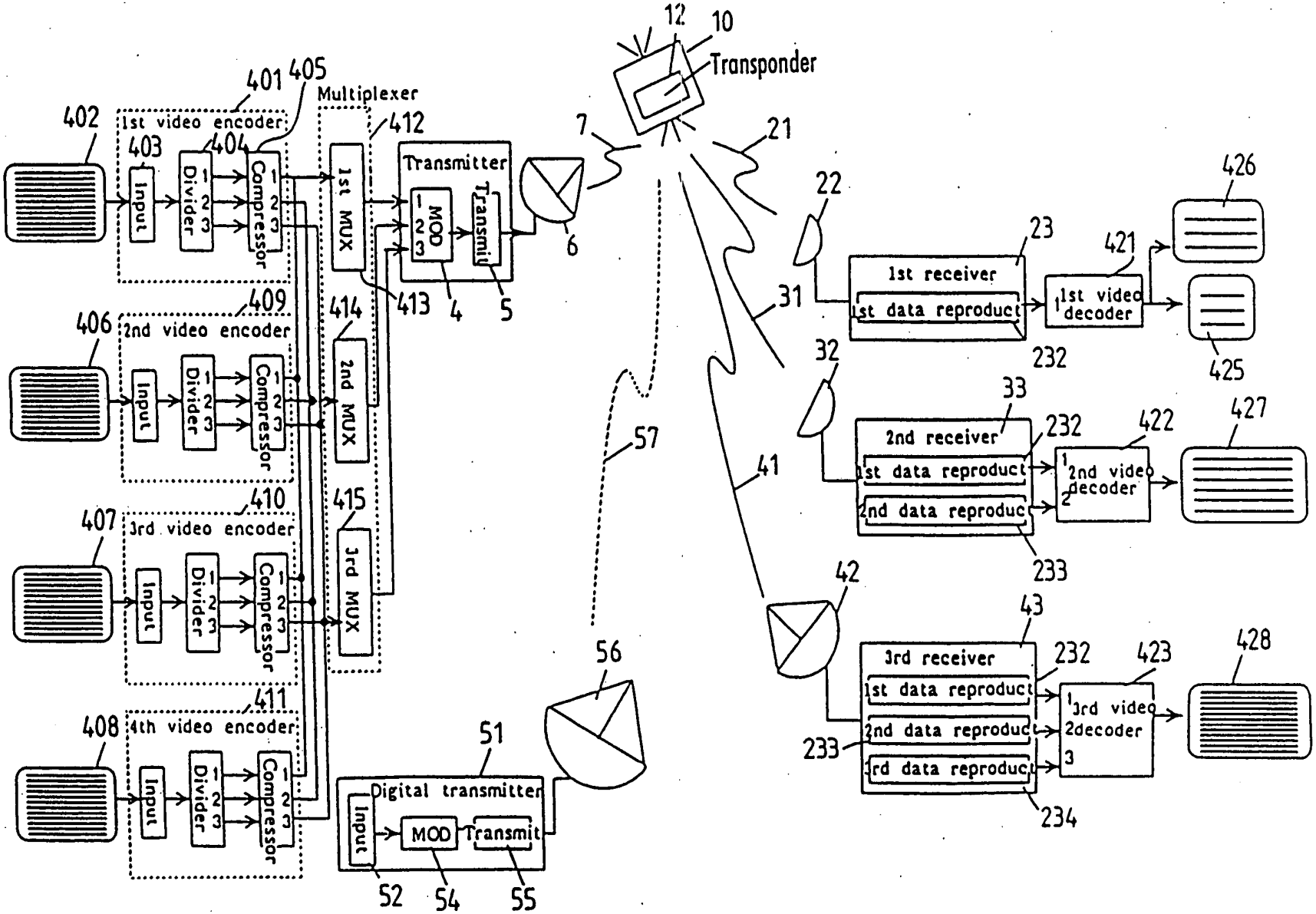

12
10
Transponder
401
405
Multiplexer
402
1st video encoder
403
404
412
Transmitter
7
21
Input
Divider
Compressor
1st MUX
MOD
Transmit
6
22
426
23
421
1st receiver
1st video decoder
31
1st data reproduct
232
425
413
4
5
406
409
414
32
33
2nd video encoder
2nd receiver
232
422
427
2nd MUX
41
1st data reproduct
2nd video decoder
2nd data reproduc
57
233
407
410
415
42
43
3rd video encoder
3rd receiver
232
423
428
3rd MUX
1st data reproduct
3rd video decoder
2nd data reproduc
233
3rd data reproduc
234
56
408
411
4th video encoder
51
Digital transmitter
Input
MOD
Transmit
52
54
55

FIG. 30

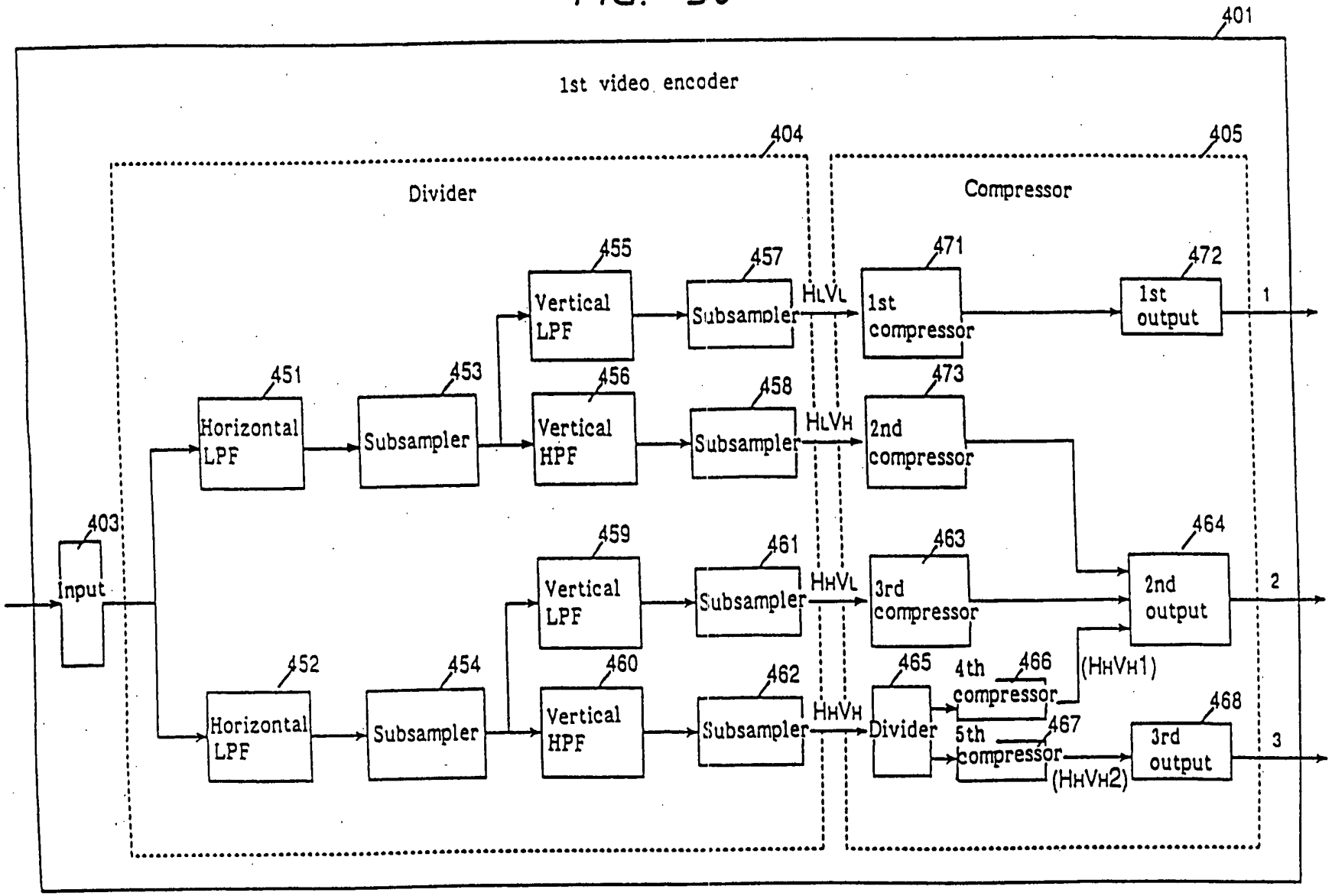

401
1st video encoder
404
Divider
405
Compressor
403
Input
451
Horizontal LPF
453
Subsampler
455
Vertical LPF
456
Vertical HPF
457
Subsampler
458
Subsampler
HLVL
HLVH
471
1st compressor
472
1st output
1
473
2nd compressor
459
Vertical LPF
460
Vertical HPF
461
Subsampler
462
Subsampler
HHVL
HHVH
463
3rd compressor
464
2nd output
2
452
Horizontal LPF
454
Subsampler
465
Divider
4th compressor
466
(HHVH1)
5th compressor
467
(HHVH2)
468
3rd output
3

FIG. 31

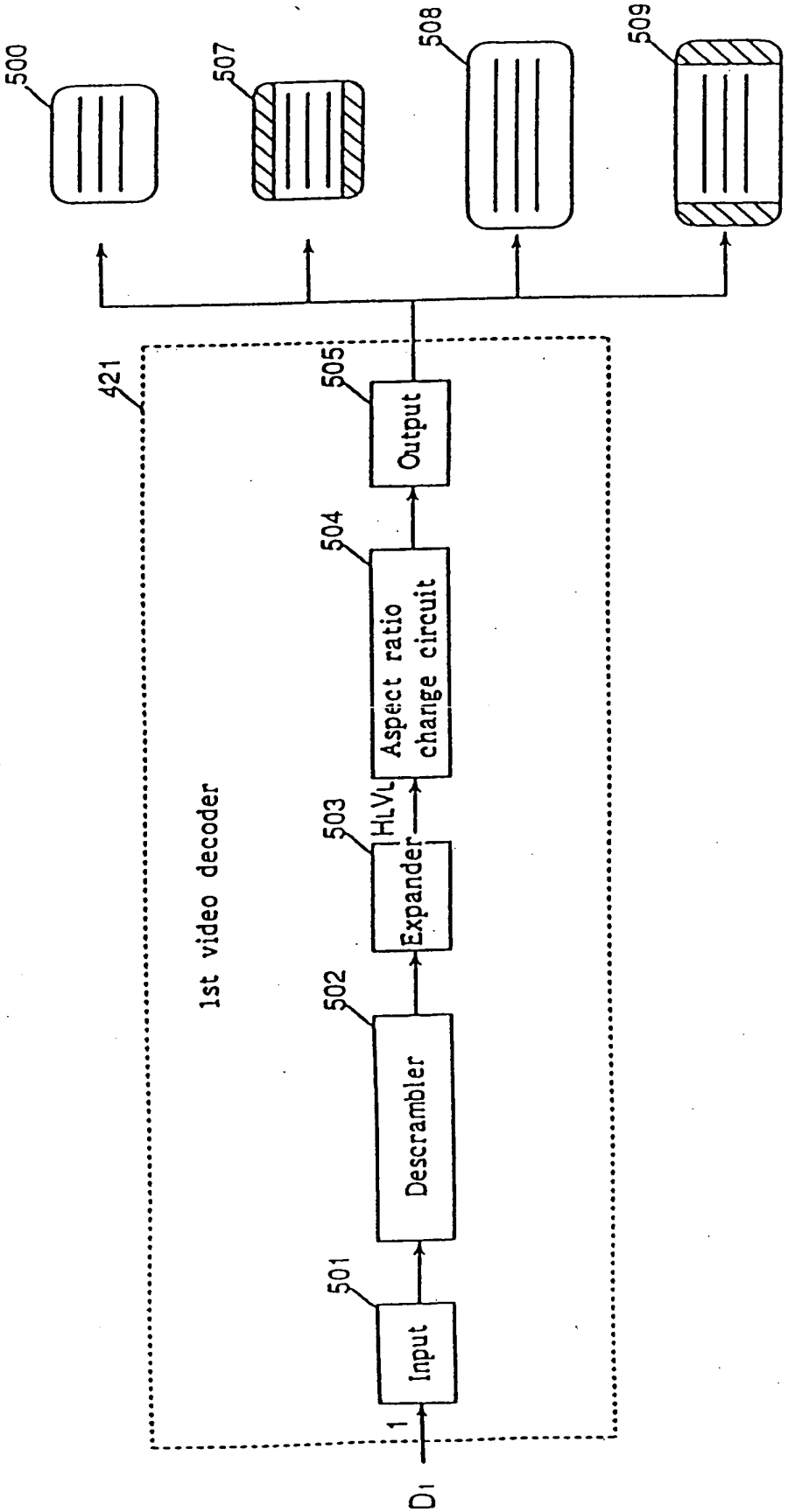

500
507
508
509
421
505
Output
504
Aspect ratio change circuit
503
HLVL
Expander
502
Descrambler
501
Input
1
D1
1st video decoder

FIG. 32

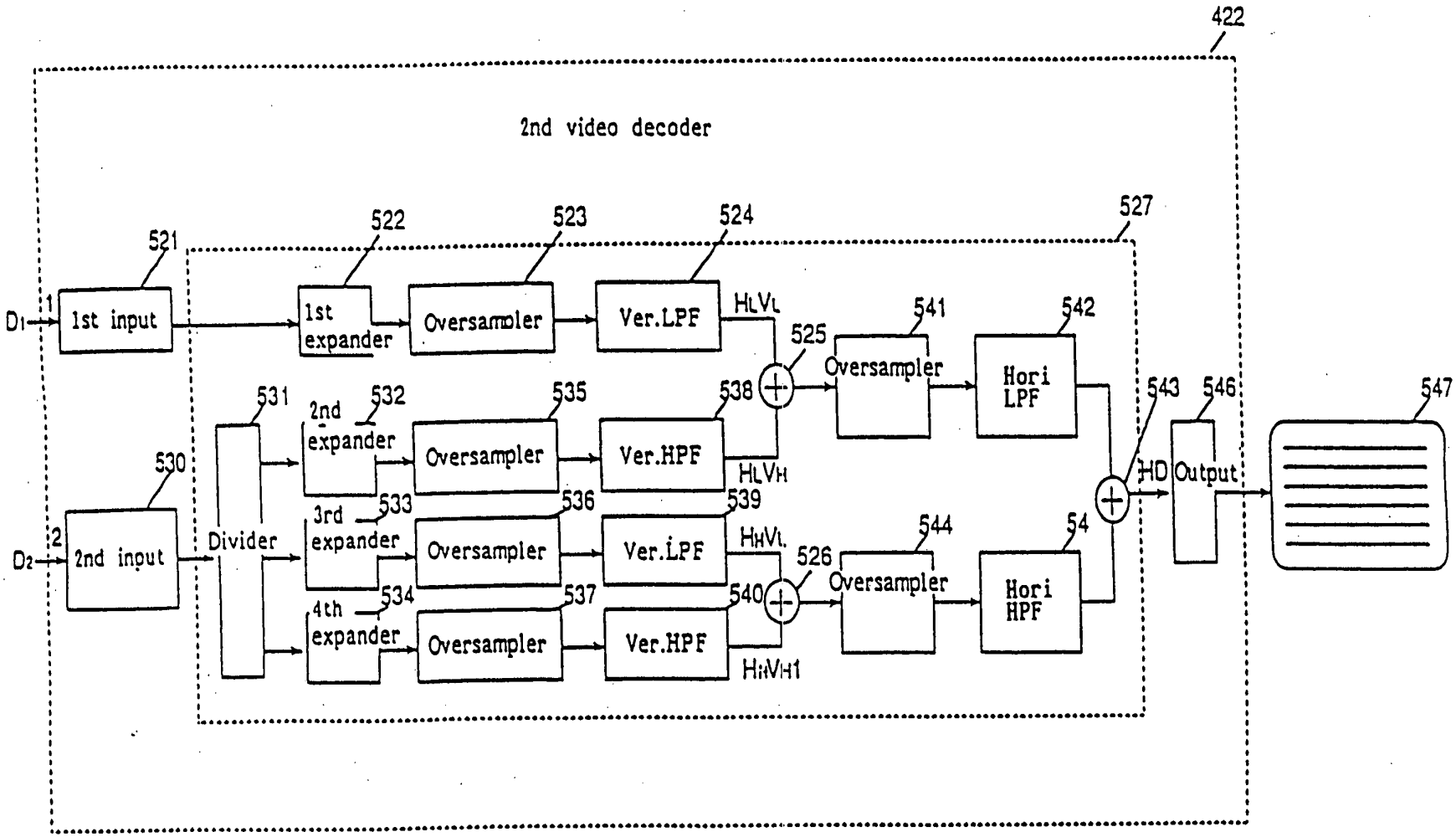

422
2nd video decoder
521
522
523
524
527
D1
1
1st input
1st expander
Oversampler
Ver.LPF
HLVL
525
541
542
Oversampler
Hori LPF
531
2nd expander
532
535
538
543
546
547
530
Oversampler
Ver.HPF
HLVH
HD
Output
2
D2
2nd input
Divider
3rd expander
533
536
539
Oversampler
Ver.LPF
HHVL
526
544
54
Oversampler
Hori HPF
4th expander
534
537
540
Oversampler
Ver.HPF
HHVH1

FIG. 33

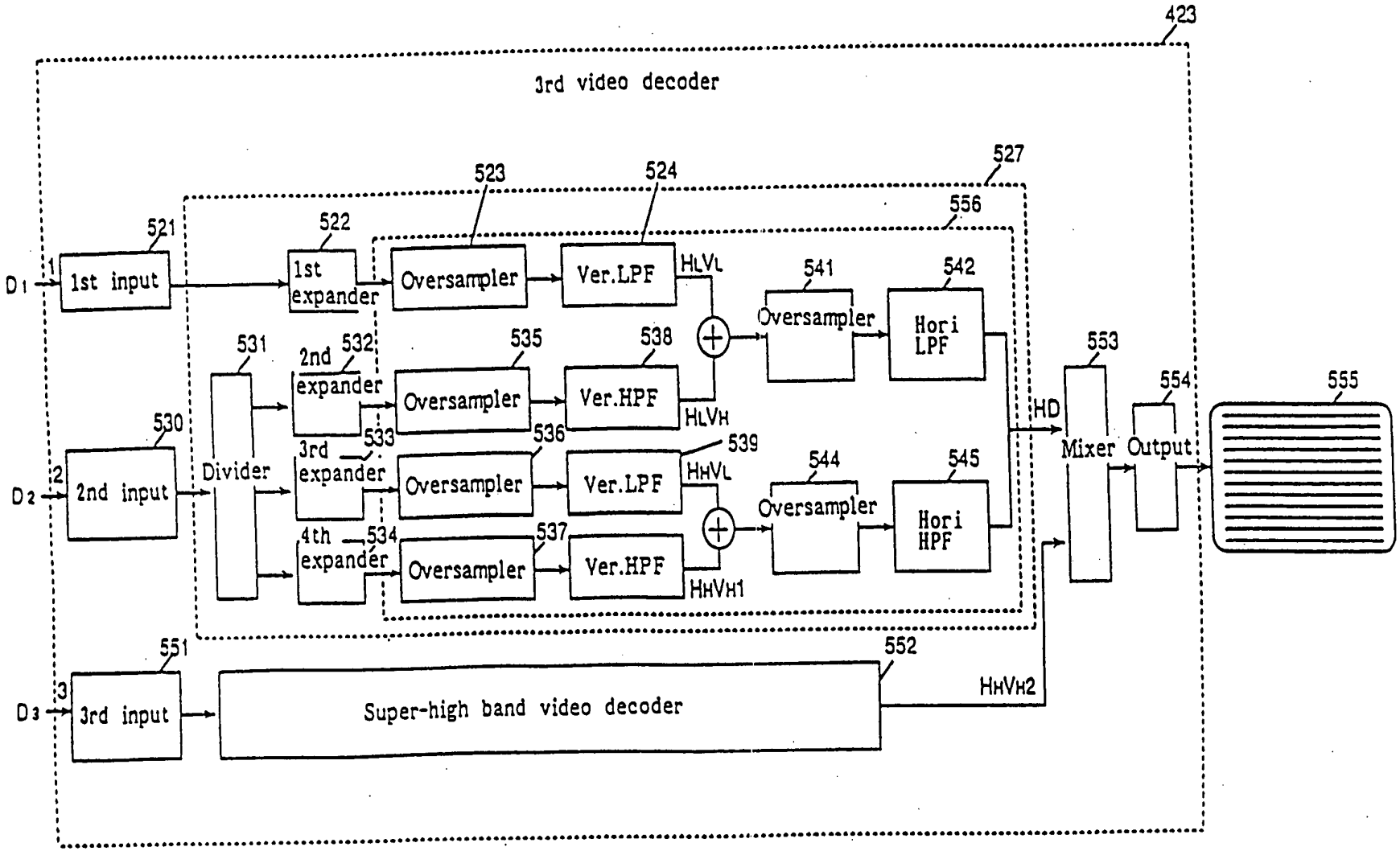

423
3rd video decoder
527
523
524
556
521
522
1st input
1st expander
Oversampler
Ver.LPF
HLVL
541
542
Oversampler
Hori LPF
D1
1
531
2nd 532
expander
535
538
Oversampler
Ver.HPF
HLVH
553
554
555
530
533
536
539
HD
2nd input
Divider
3rd expander
Oversampler
Ver.LPF
HHVL
544
545
Mixer
Output
D2
2
4th 534
expander
537
Oversampler
Ver.HPF
HHVH1
Hori HPF
551
552
3
D3
3rd input
Super-high band video decoder
HHVH2

FIG. 34

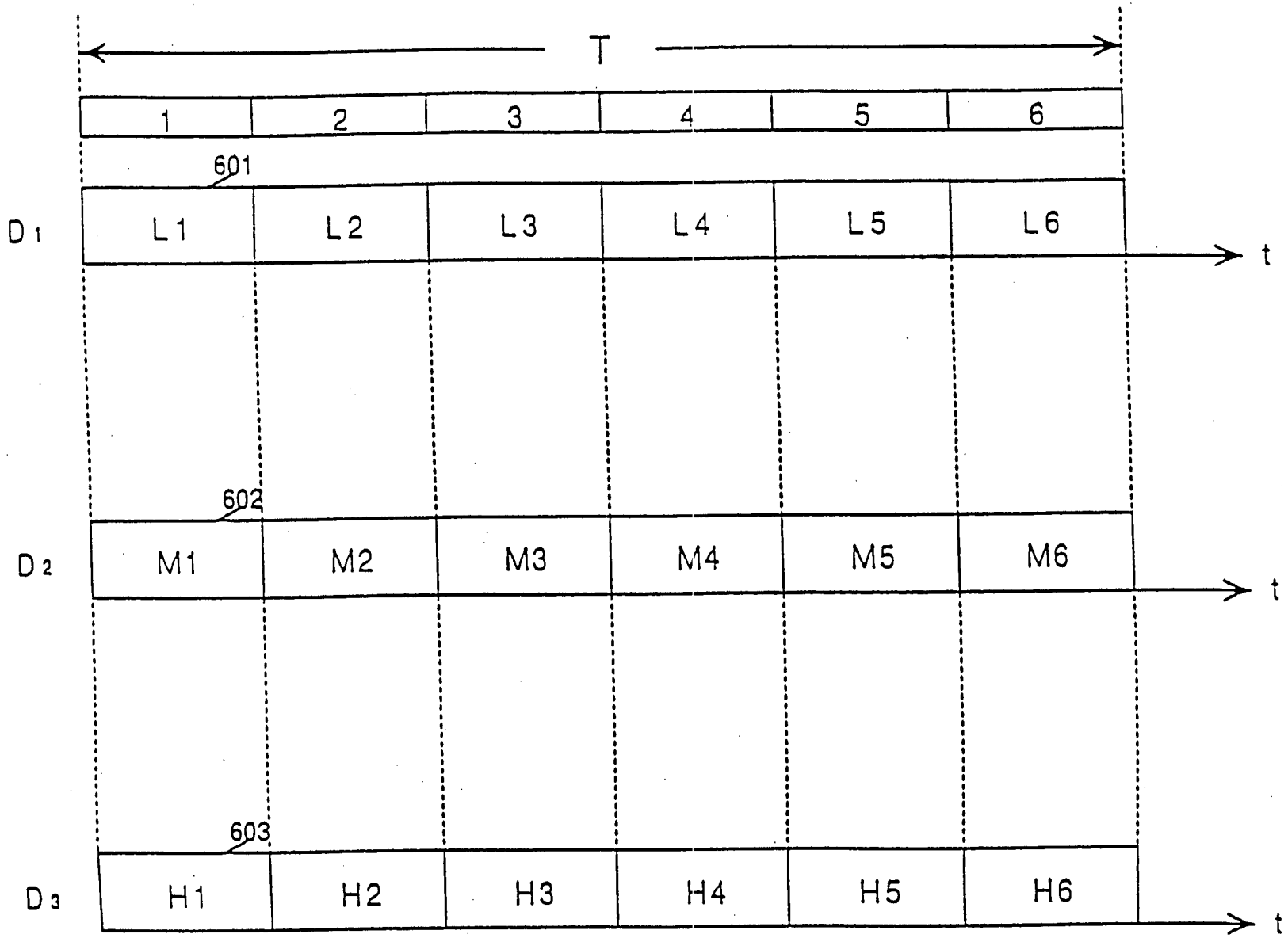

T
1
2
3
4
5
6
601
D1
L1
L2
L3
L4
L5
L6
t
602
D2
M1
M2
M3
M4
M5
M6
t
603
D3
H1
H2
H3
H4
H5
H6
t

FIG. 35

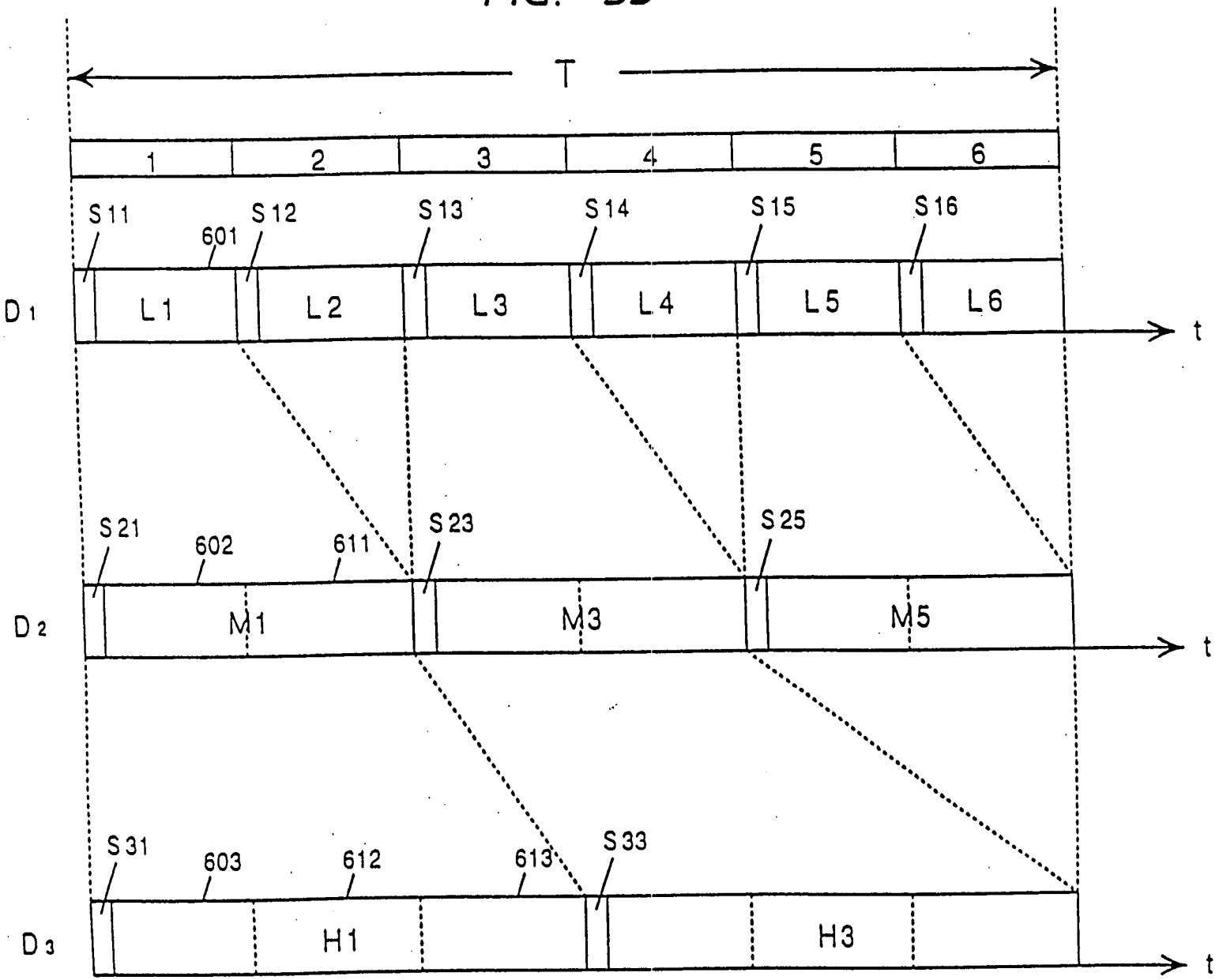

T
1
2
3
4
5
6
S11
S12
S13
S14
S15
S16
601
D1
L1
L2
L3
L4
L5
L6
t
S21
602
611
S23
S25
D2
M1
M3
M5
t
S31
603
612
613
S33
D3
H1
H3
t

FIG. 36

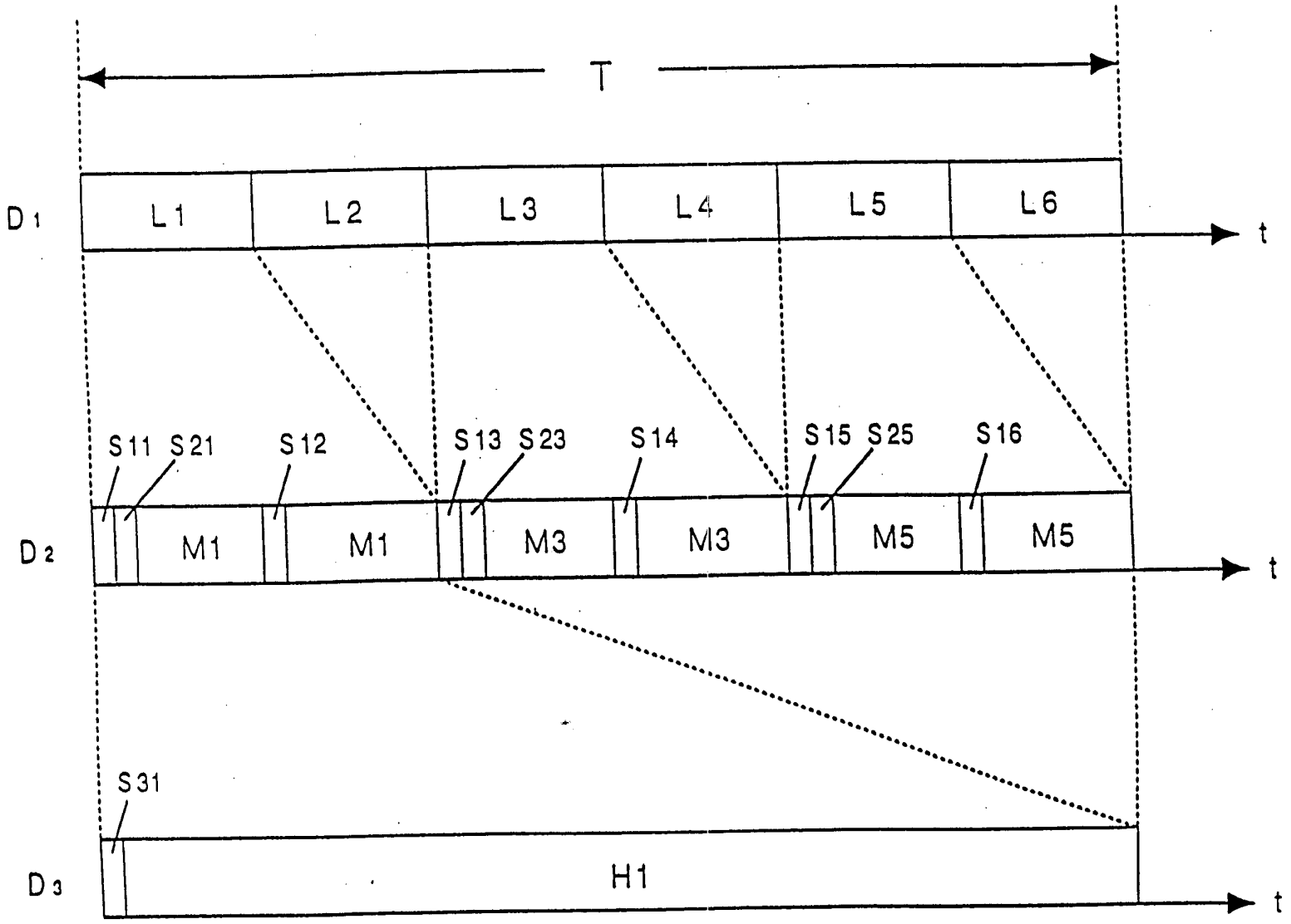

T
D1
L1
L2
L3
L4
L5
L6
t
S11 S21
S12
S13 S23
S14
S15 S25
S16
D2
M1
M1
M3
M3
M5
M5
t
S31
D3
H1
t

FIG. 37

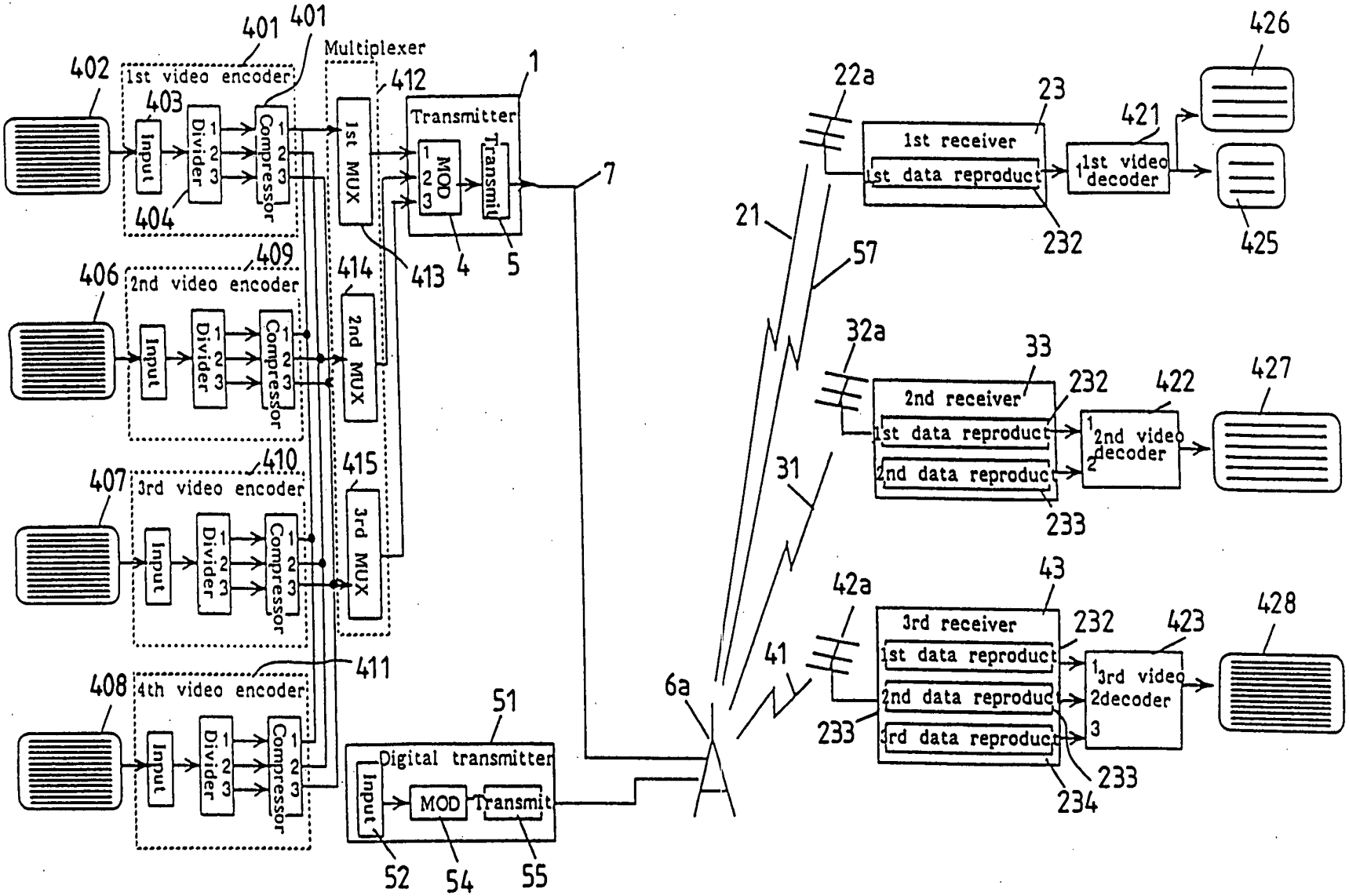

401
401
Multiplexer
402
1st video encoder
403
Input
Divider
Compressor
404
412
1st MUX
Transmitter
MOD
Transmit
1
7
4
5
413
406
409
2nd video encoder
414
2nd MUX
407
410
3rd video encoder
415
3rd MUX
408
411
4th video encoder
51
Digital transmitter
52
54
55
6a
21
57
31
41
22a
23
1st receiver
1st data reproduct
232
421
1st video decoder
426
425
32a
33
2nd receiver
232
422
2nd video decoder
427
233
42a
43
3rd receiver
232
423
3rd video decoder
428
233
234

FIG. 38

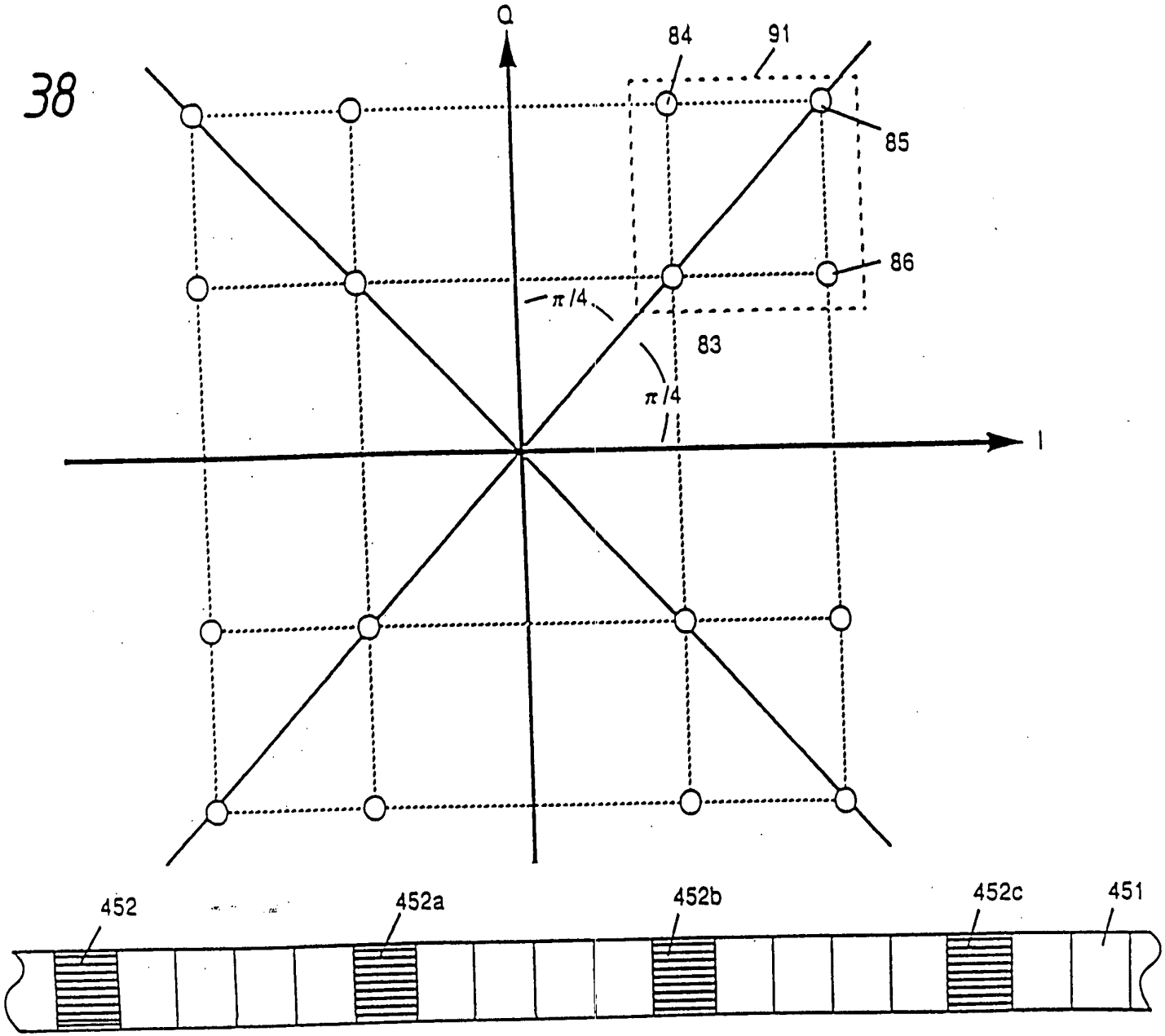


FIG. 39

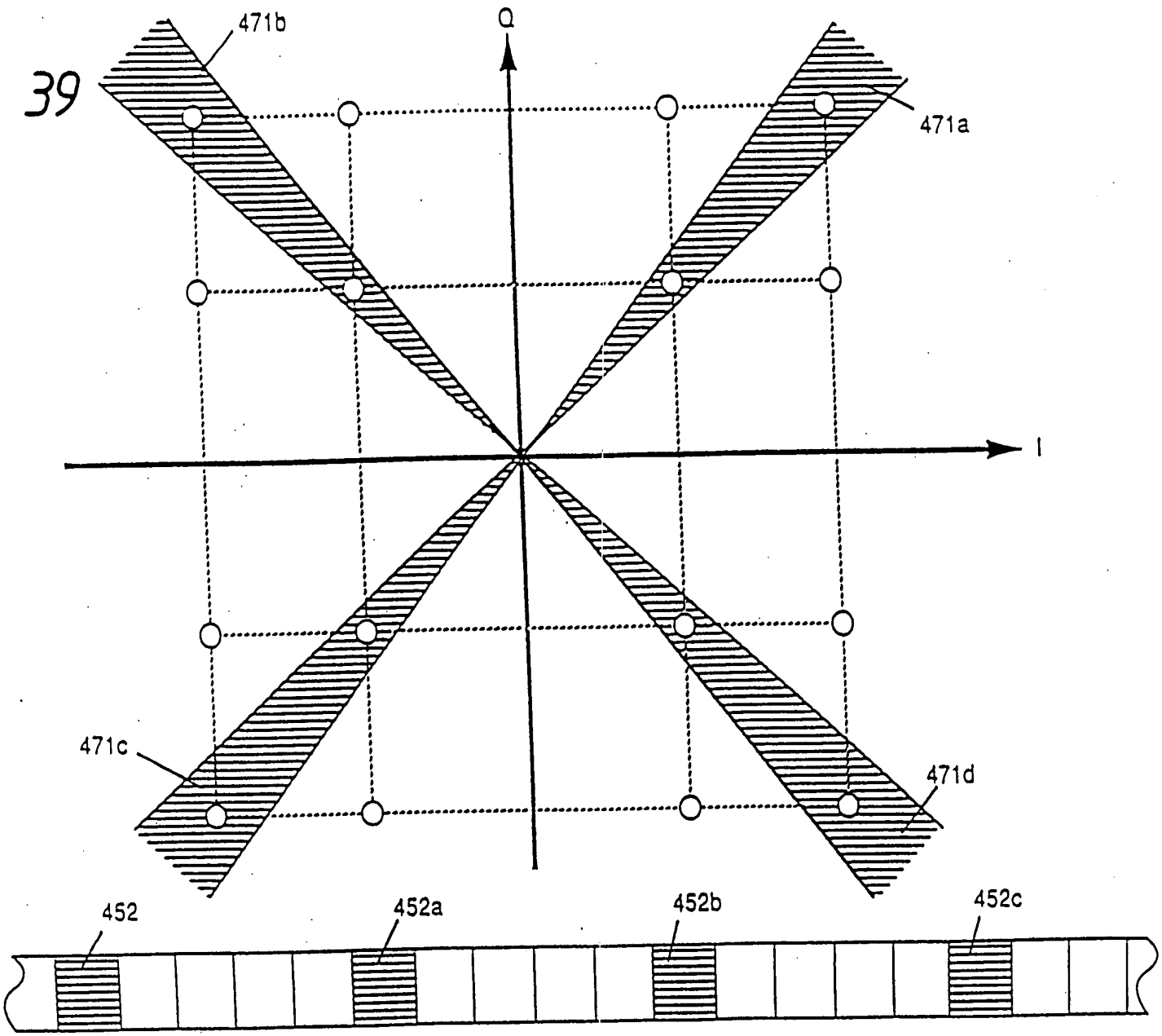


FIG. 40

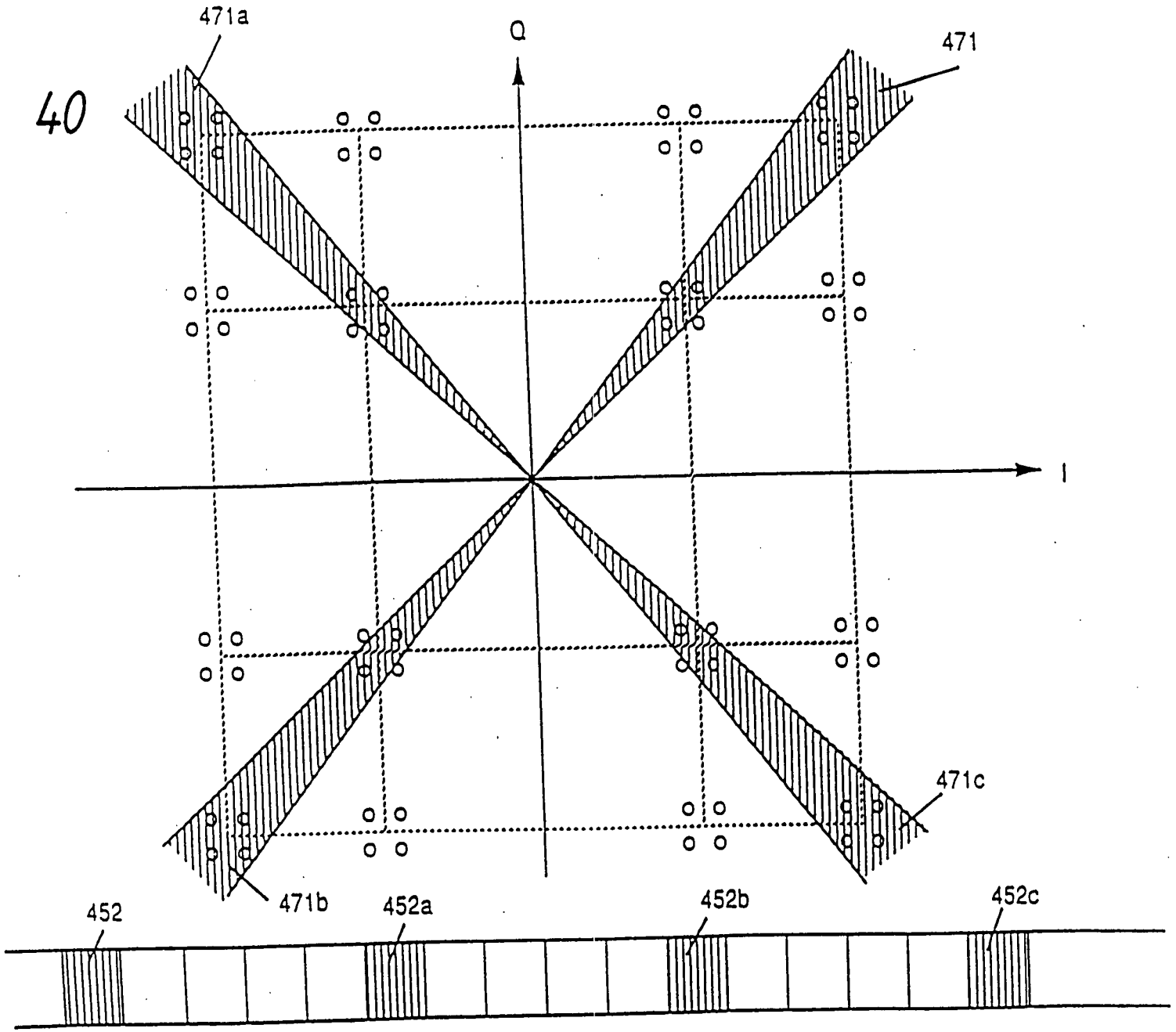


FIG. 41

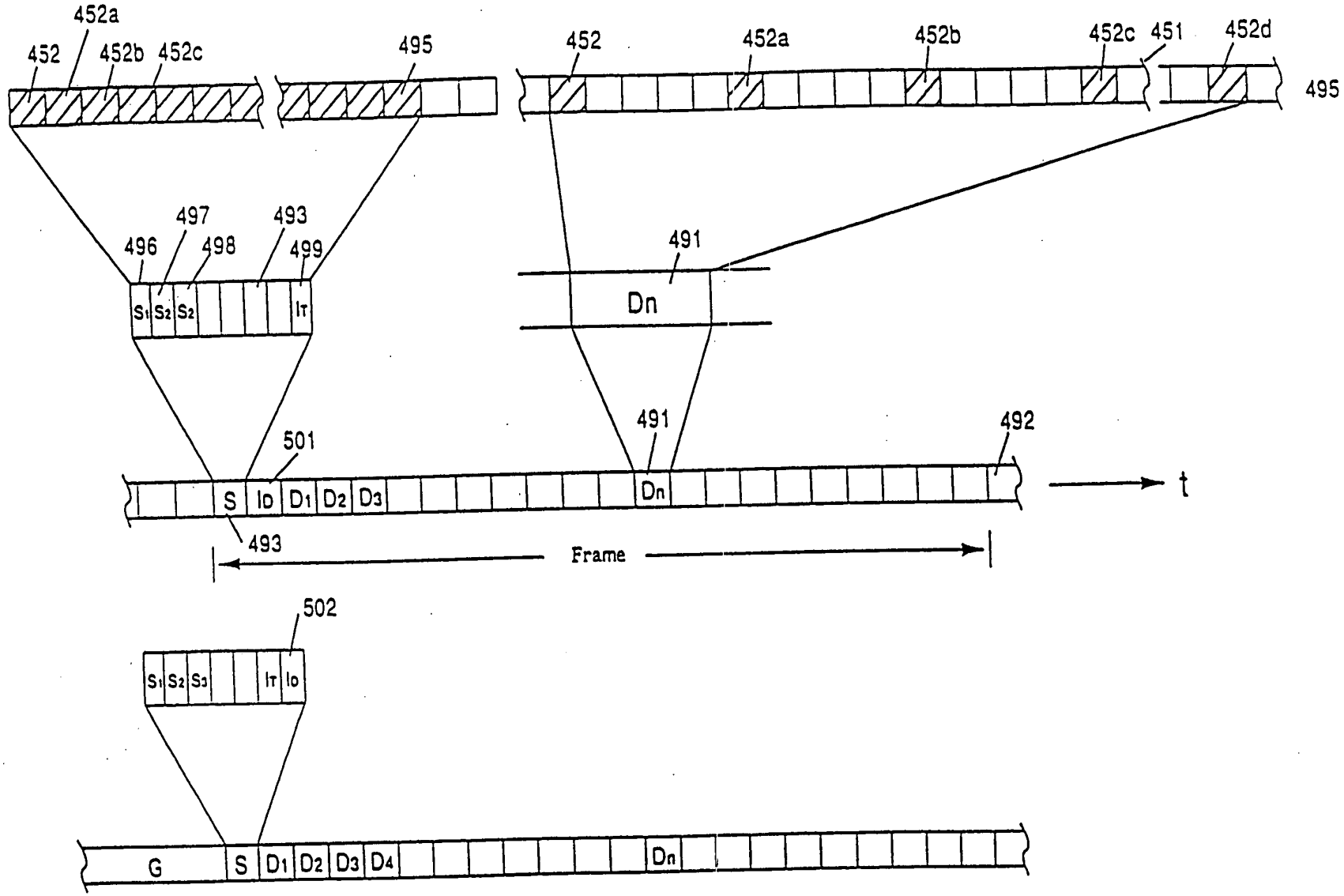

452a
452
452b
452c
495
452
452a
452b
452c
451
452d
495
497
493
496
498
499
491
S1 S2 S2
IT
Dn
491
492
501
S
ID
D1
D2
D3
Dn
t
493
Frame
502
S1 S2 S3
IT
IO
G
S
D1
D2
D3
D4
Dn

FIG. 42

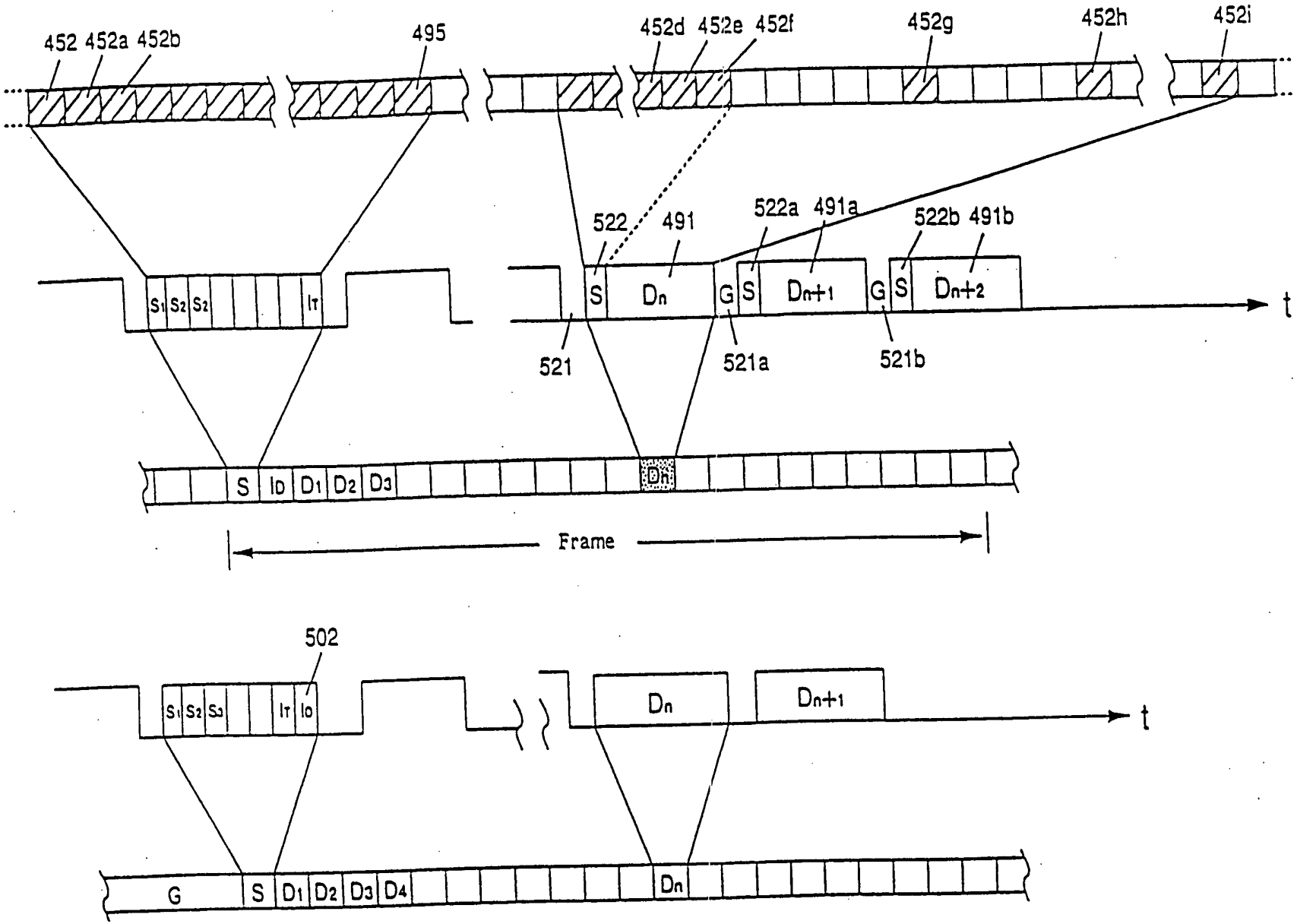

452 452a 452b
495
452d 452e 452f
452g
452h
452i
522
491
522a 491a
522b 491b
S1 S2 S2 IT
S Dn G S Dn+1 G S Dn+2
t
521
521a
521b
S ID D1 D2 D3
Dn
Frame
502
S1 S2 S3 IT ID
Dn
Dn+1
t
G S D1 D2 D3 D4
Dn

FIG. 43

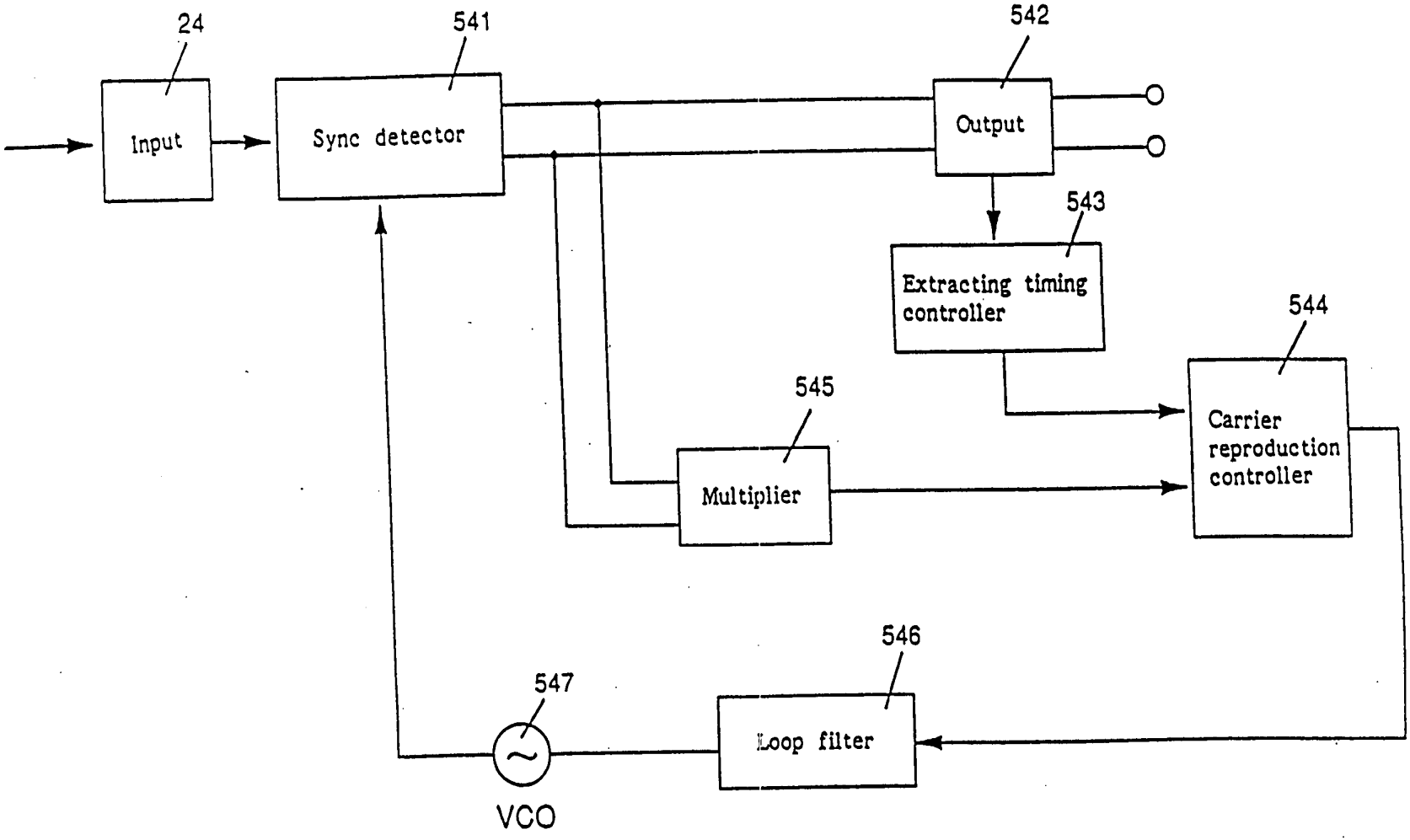

24
541
542
Input
Sync detector
Output
543
Extracting timing controller
544
545
Carrier reproduction controller
Multiplier
546
547
Loop filter
VCO

FIG. 44

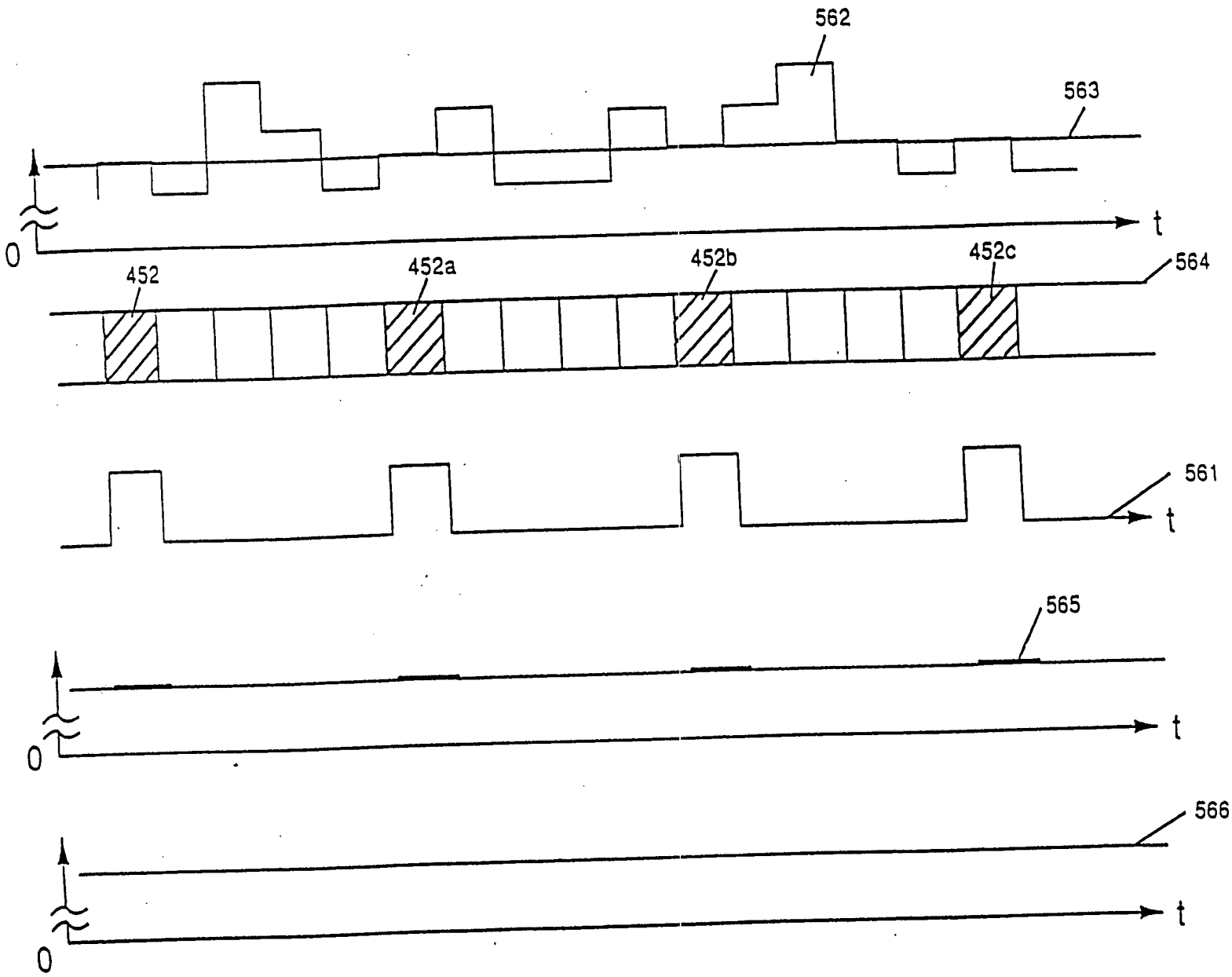


FIG. 45

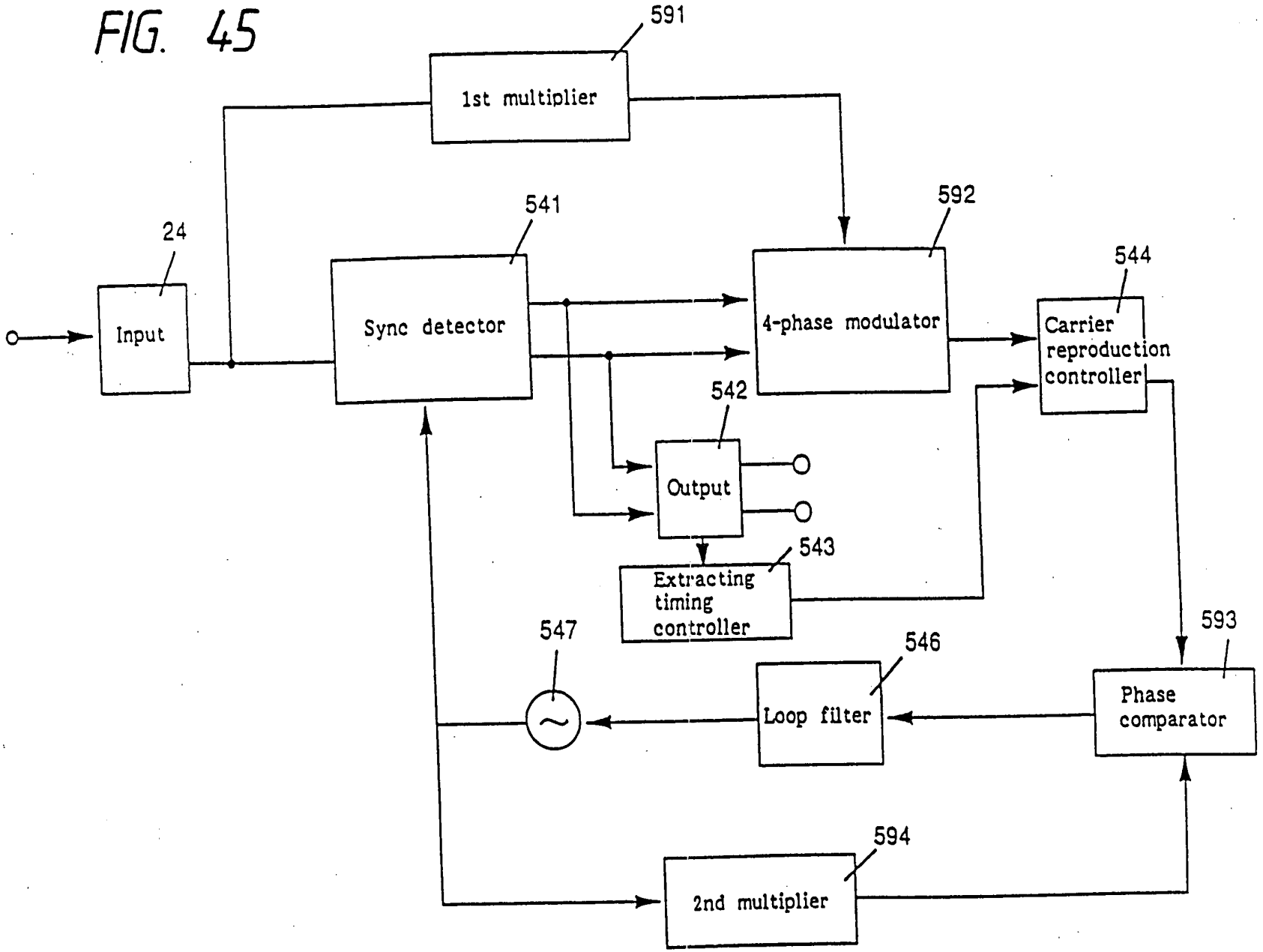

591
1st multiplier
24
Input
541
Sync detector
592
4-phase modulator
544
Carrier reproduction controller
542
Output
543
Extracting timing controller
547
546
Loop filter
593
Phase comparator
594
2nd multiplier

FIG. 46

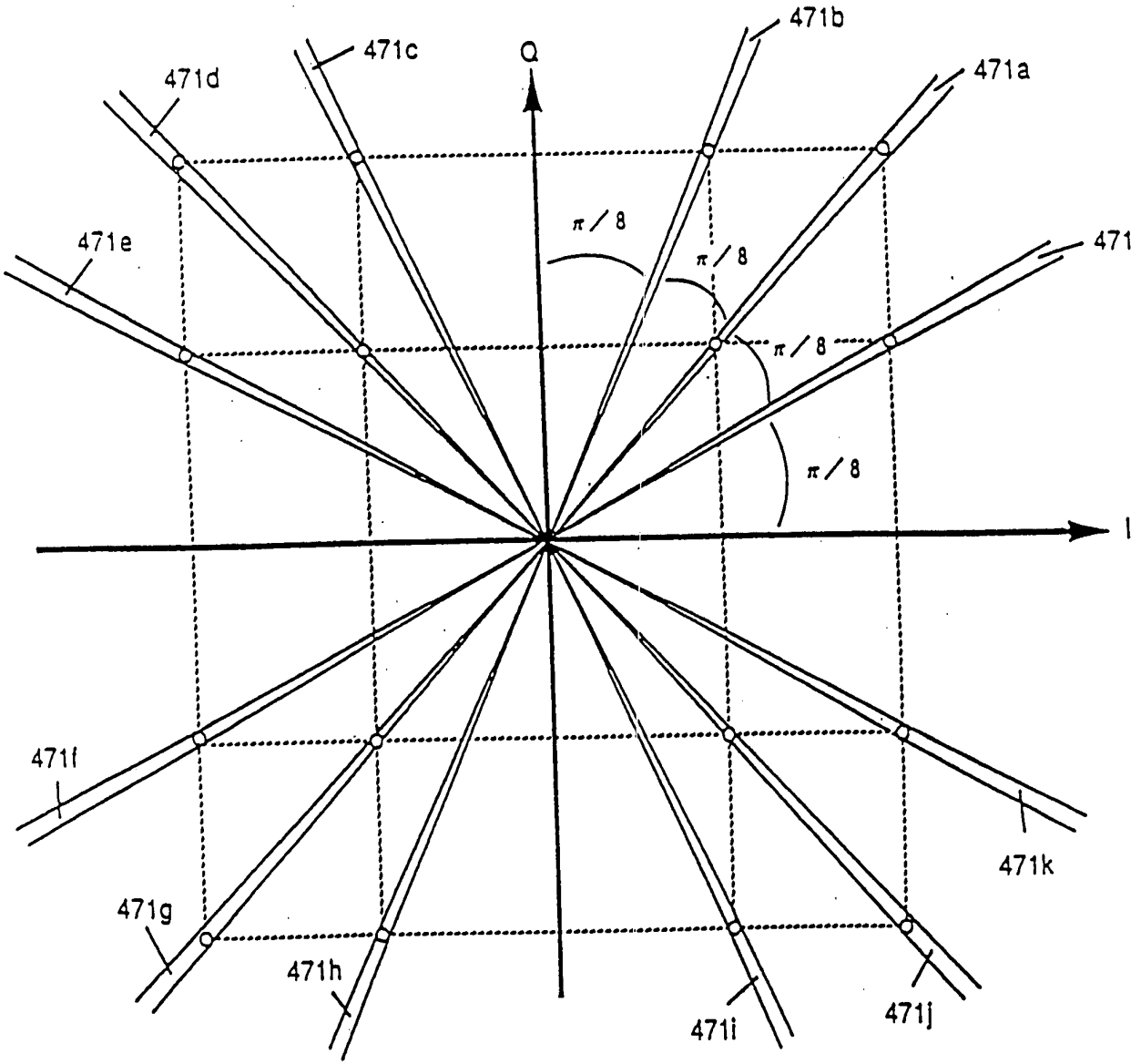

Q
I
471a
471b
471c
471d
471e
471
471f
471g
471h
471i
471j
471k
π / 8
π / 8
π / 8
π / 8

FIG. 47

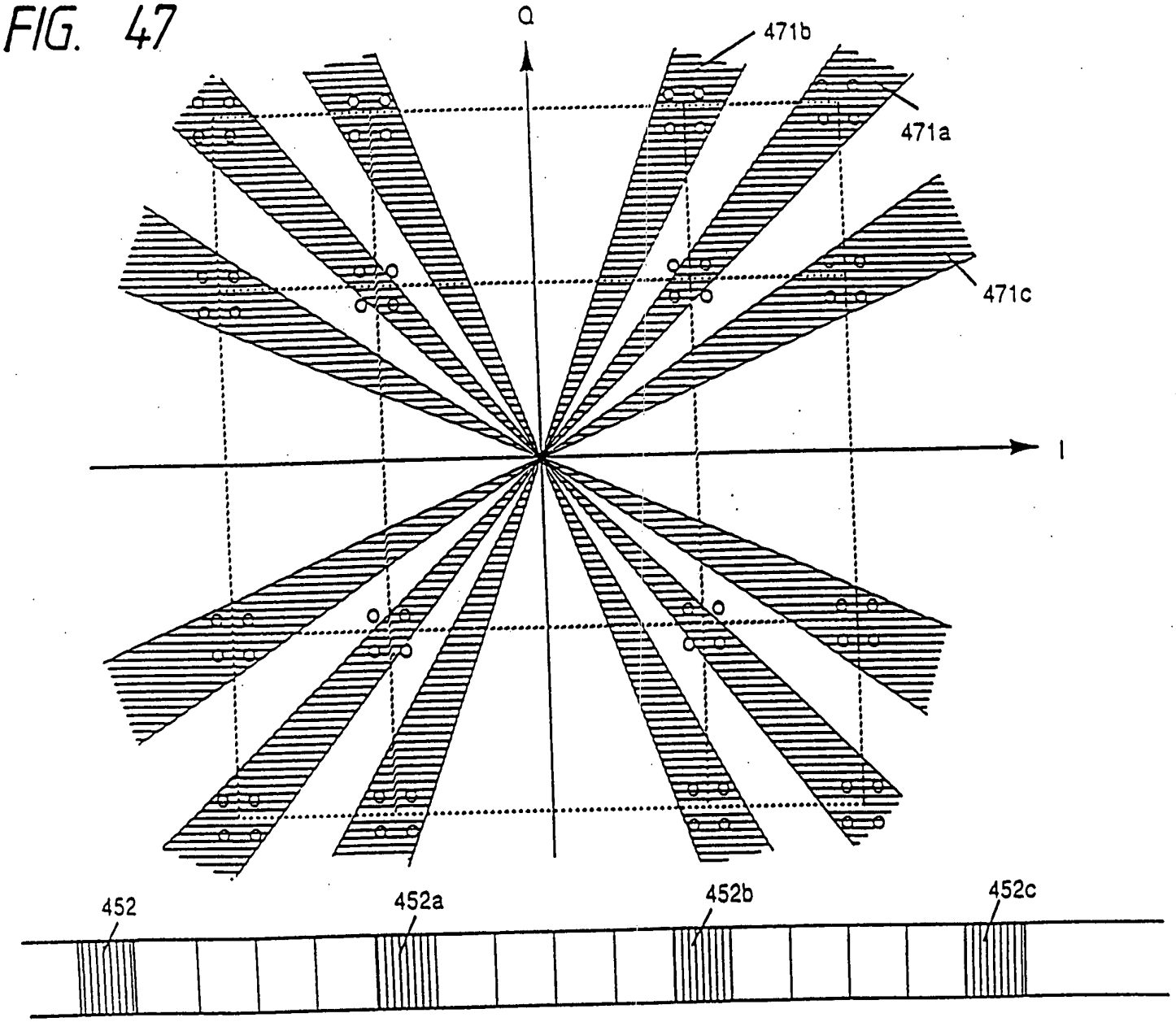


FIG. 48

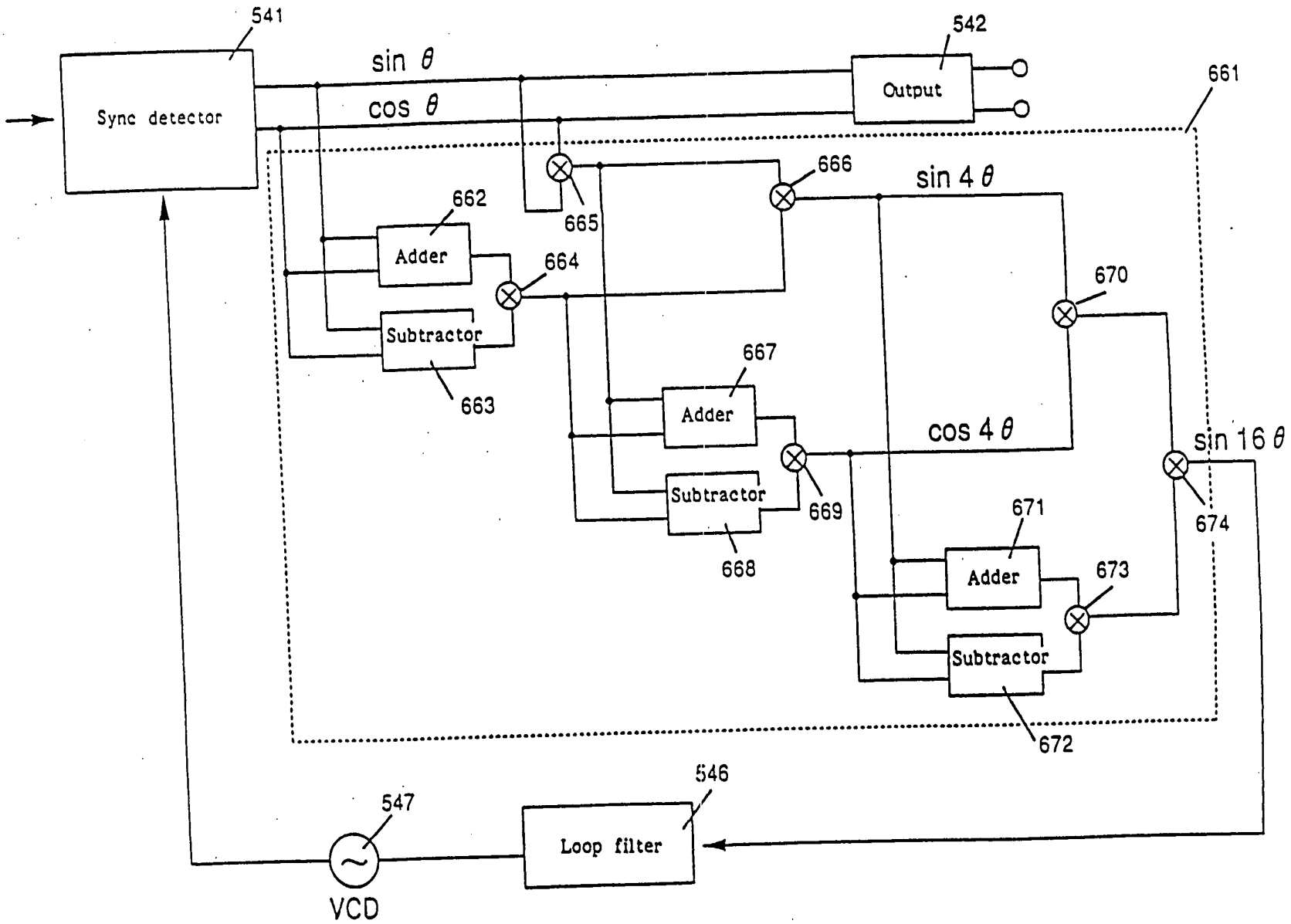

541
Sync detector
sin θ
cos θ
542
Output
661
665
666
sin 4 θ
662
Adder
664
Subtractor
663
670
667
Adder
cos 4 θ
sin 16 θ
Subtractor
668
669
671
674
Adder
673
Subtractor
672
546
547
Loop filter
VCD

FIG. 49

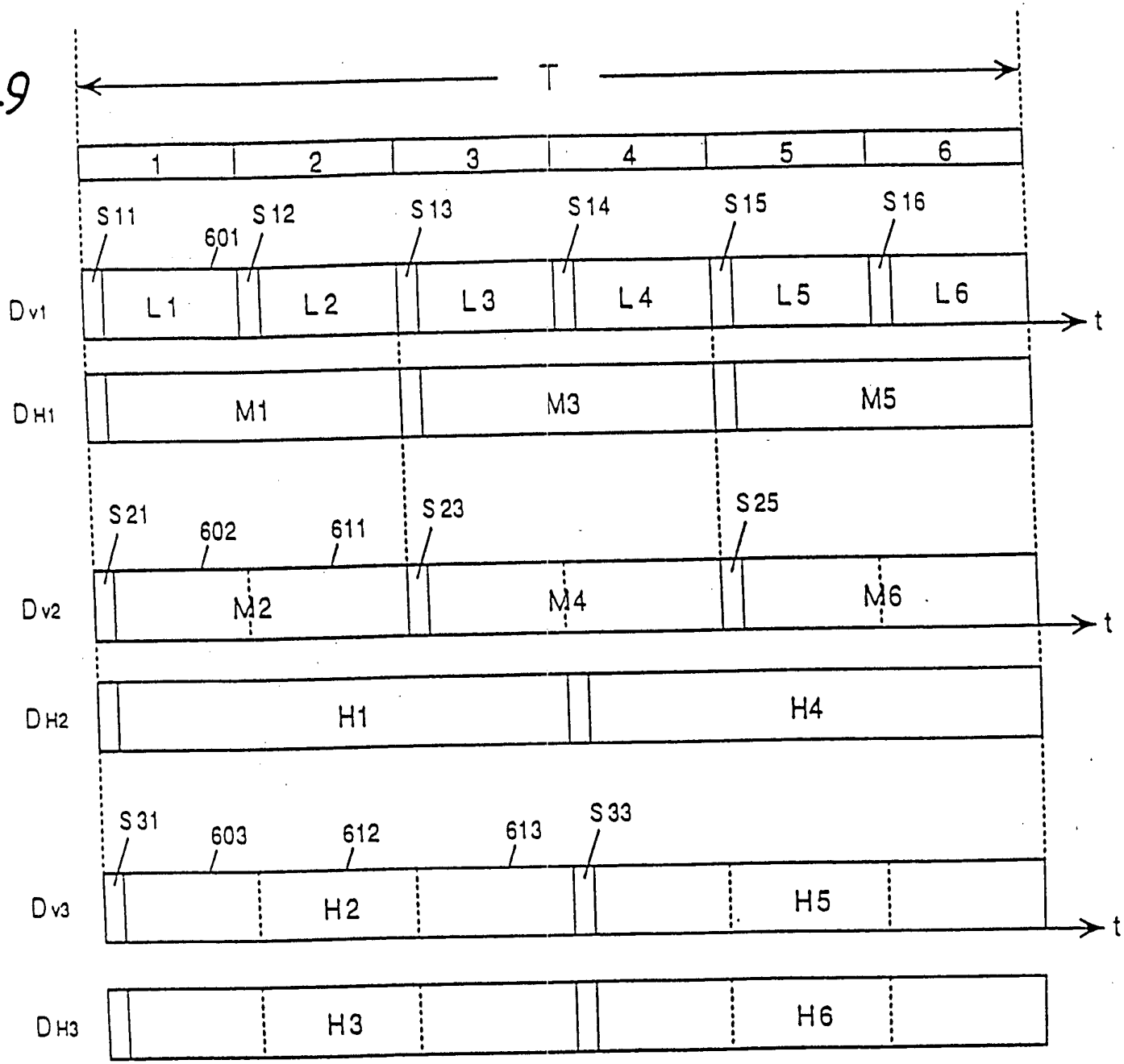

T
1
2
3
4
5
6
S11
601
S12
S13
S14
S15
S16
Dv1
L1
L2
L3
L4
L5
L6
t
DH1
M1
M3
M5
S21
602
611
S23
S25
Dv2
M2
M4
M6
t
DH2
H1
H4
S31
603
612
613
S33
Dv3
H2
H5
t
DH3
H3
H6

FIG. 50

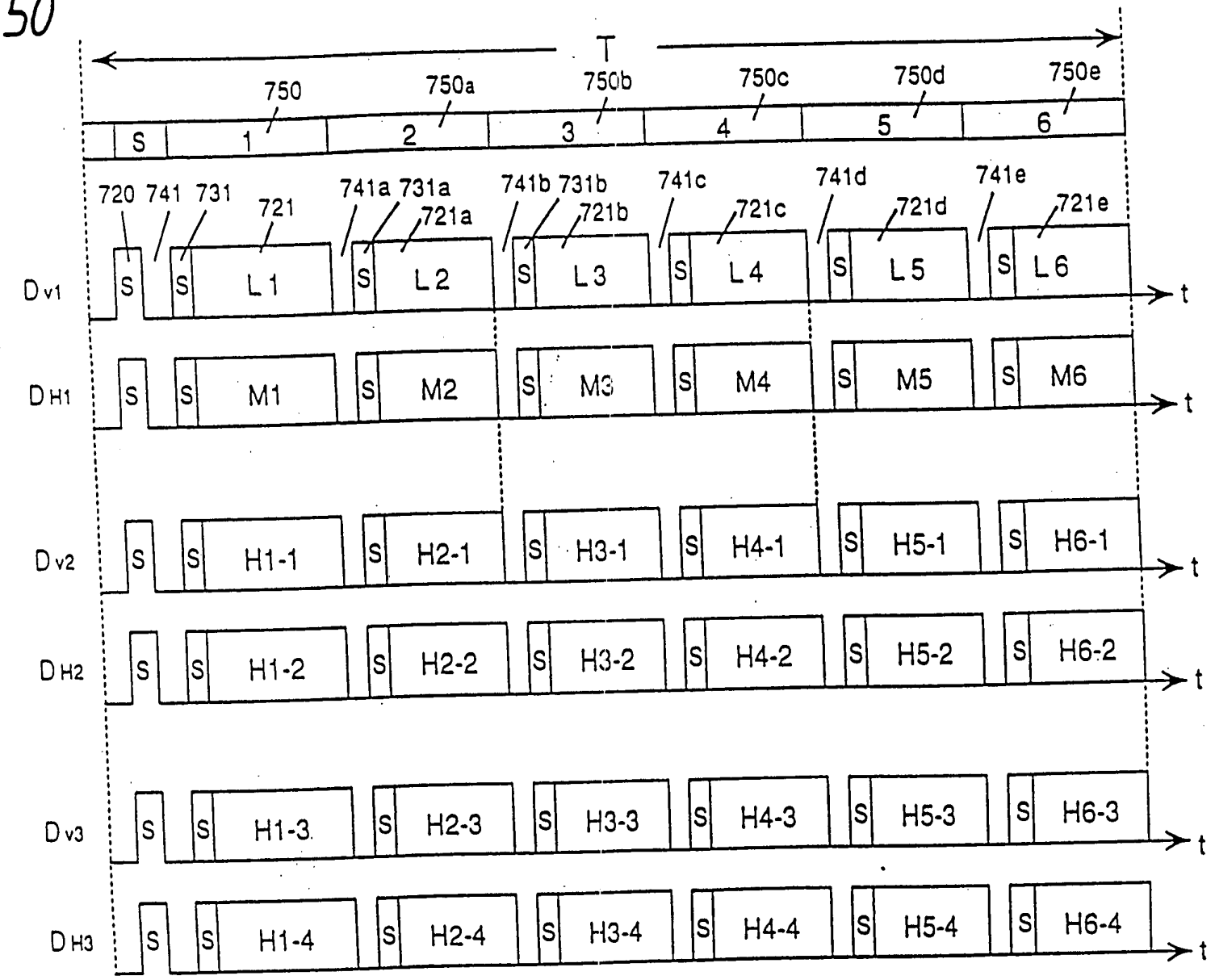

T
750
750a
750b
750c
750d
750e
S
1
2
3
4
5
6
720
741
731
721
741a
731a
721a
741b
731b
721b
741c
721c
741d
721d
741e
721e
Dv1
L1
L2
L3
L4
L5
L6
t
DH1
M1
M2
M3
M4
M5
M6
Dv2
H1-1
H2-1
H3-1
H4-1
H5-1
H6-1
DH2
H1-2
H2-2
H3-2
H4-2
H5-2
H6-2
Dv3
H1-3
H2-3
H3-3
H4-3
H5-3
H6-3
DH3
H1-4
H2-4
H3-4
H4-4
H5-4
H6-4

FIG. 51

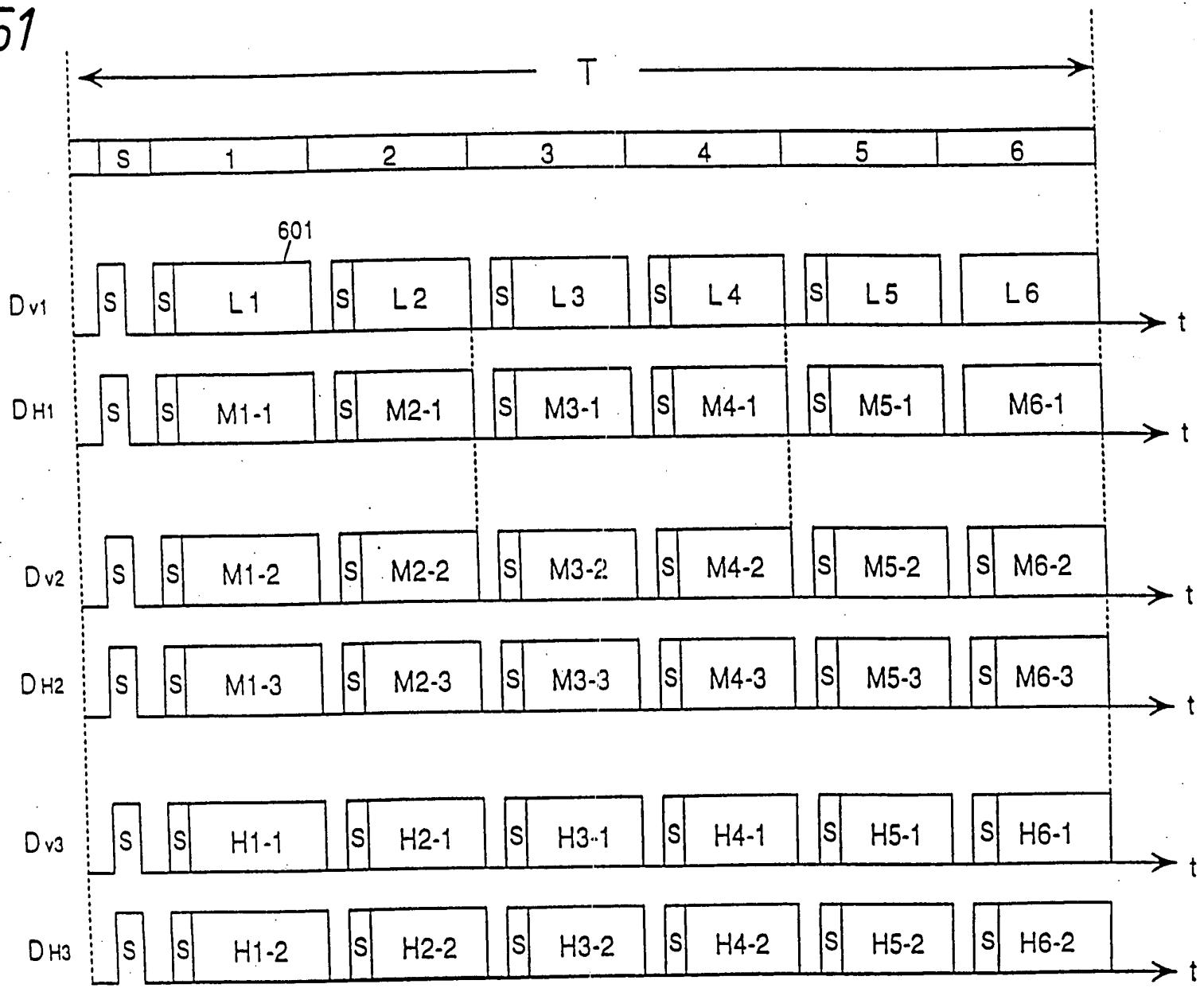

T
S
1
2
3
4
5
6
601
Dv1
DH1
Dv2
DH2
Dv3
DH3
L1
L2
L3
L4
L5
L6
M1-1
M2-1
M3-1
M4-1
M5-1
M6-1
M1-2
M2-2
M3-2
M4-2
M5-2
M6-2
M1-3
M2-3
M3-3
M4-3
M5-3
M6-3
H1-1
H2-1
H3-1
H4-1
H5-1
H6-1
H1-2
H2-2
H3-2
H4-2
H5-2
H6-2
t

FIG. 52

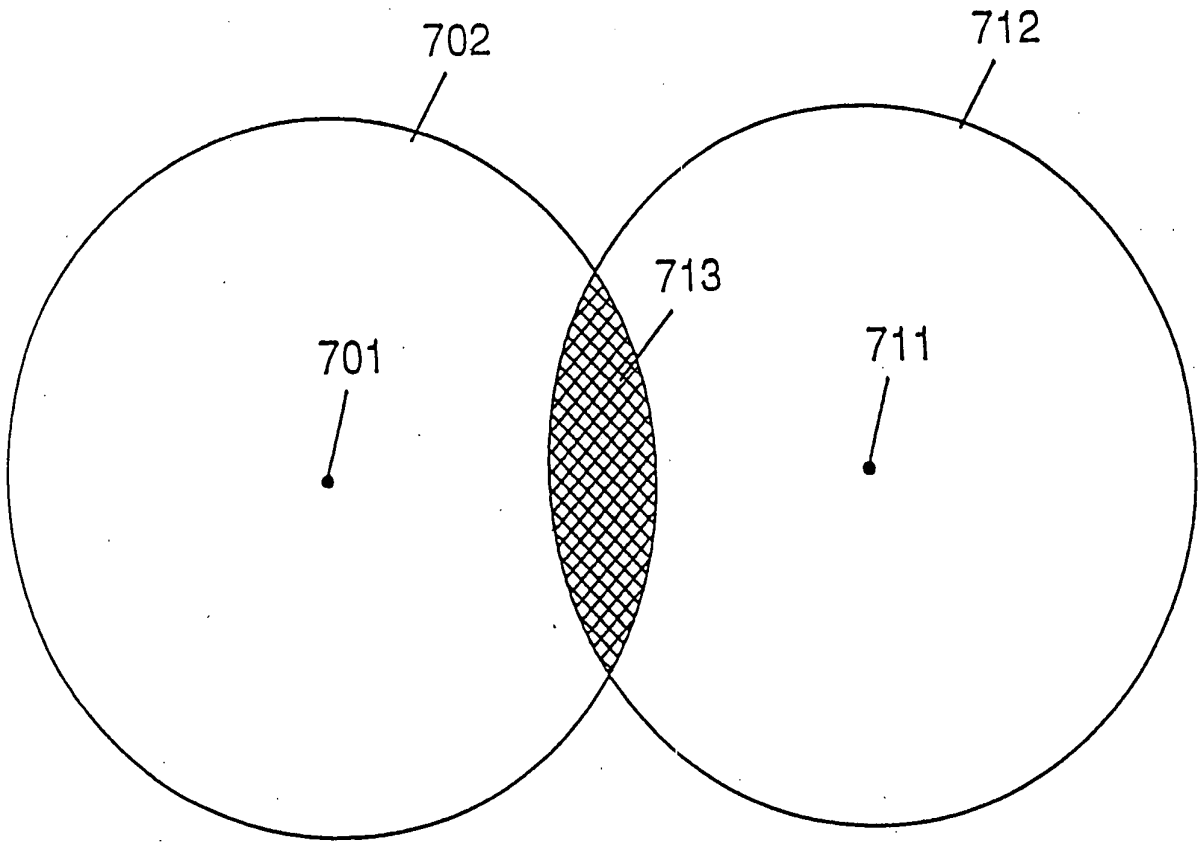


FIG. 53

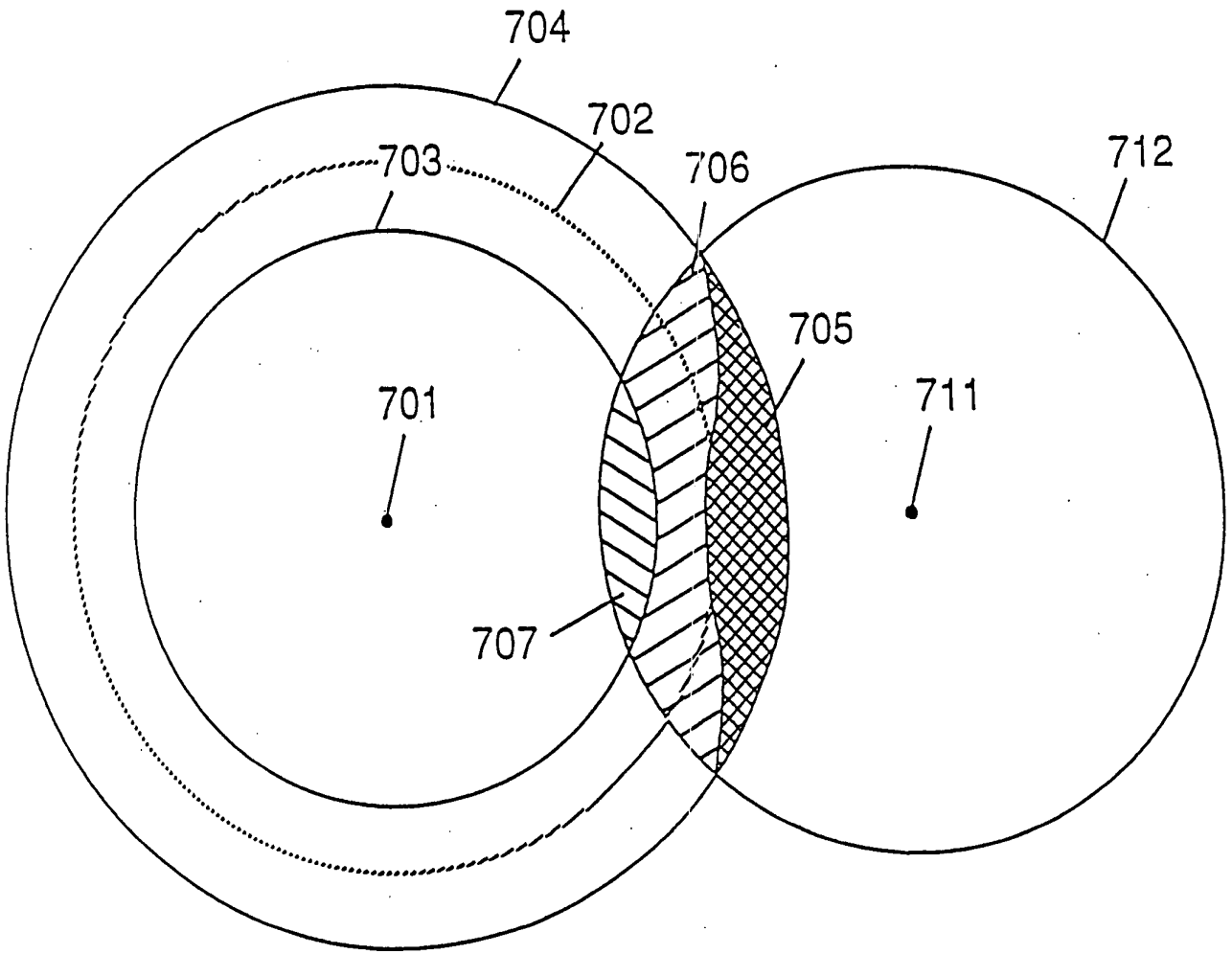


FIG. 54

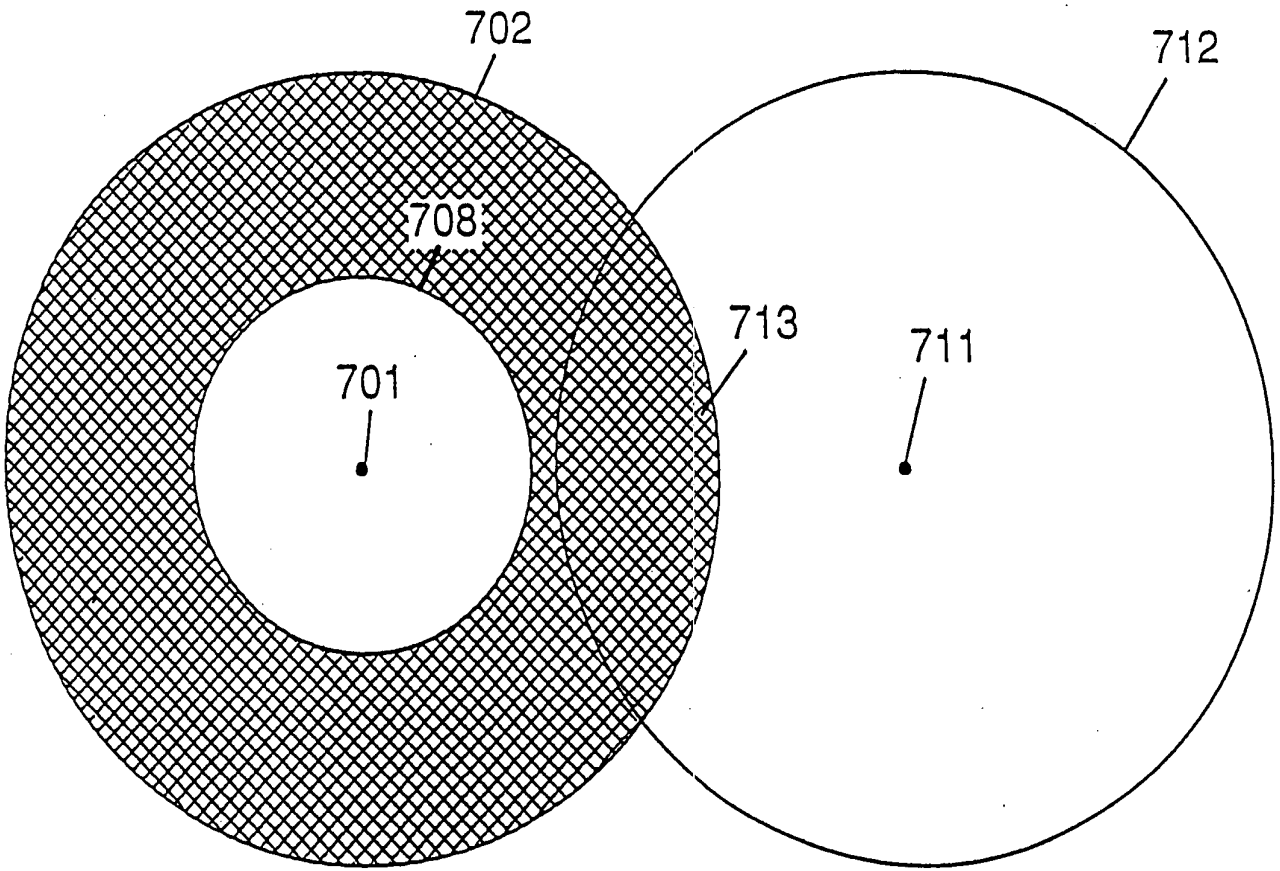


FIG. 55

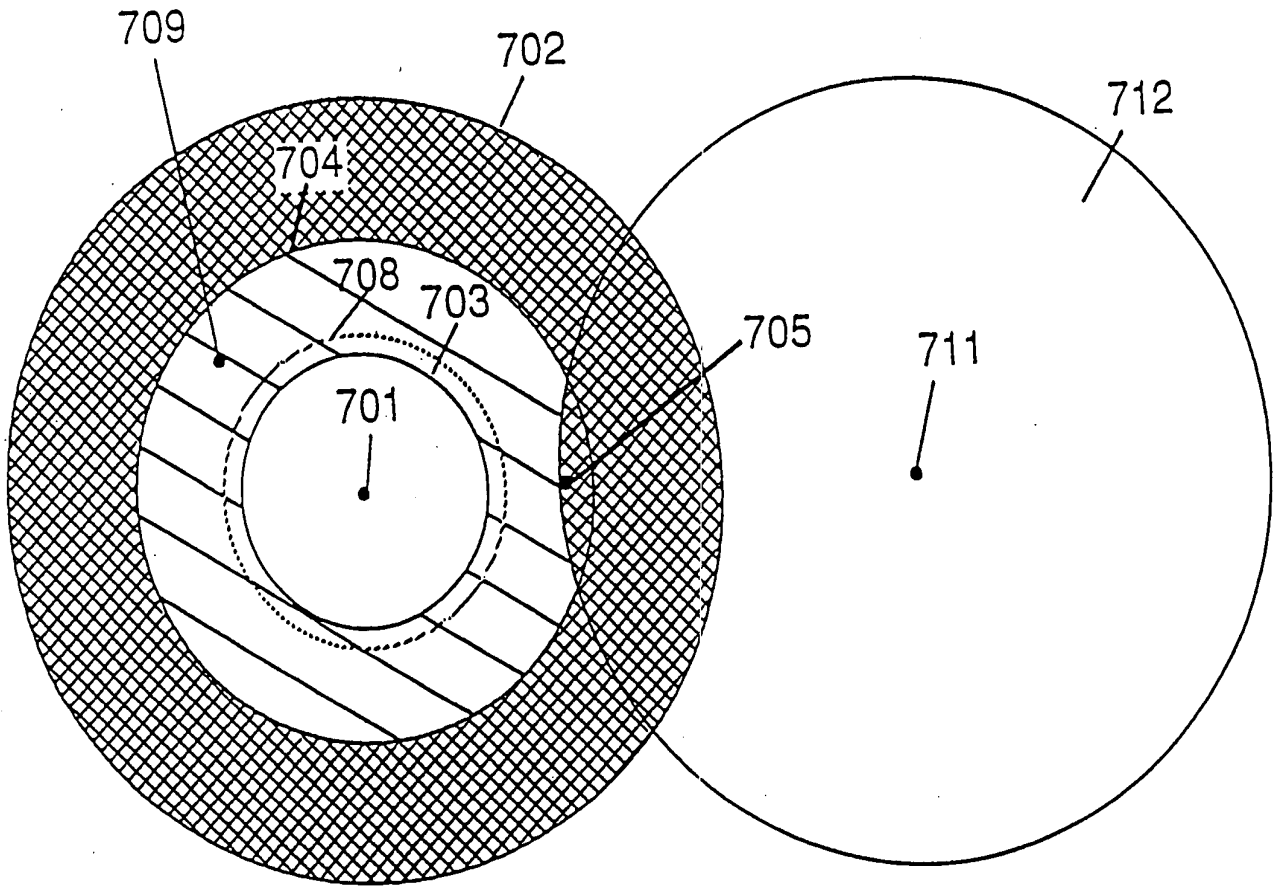


FIG. 56

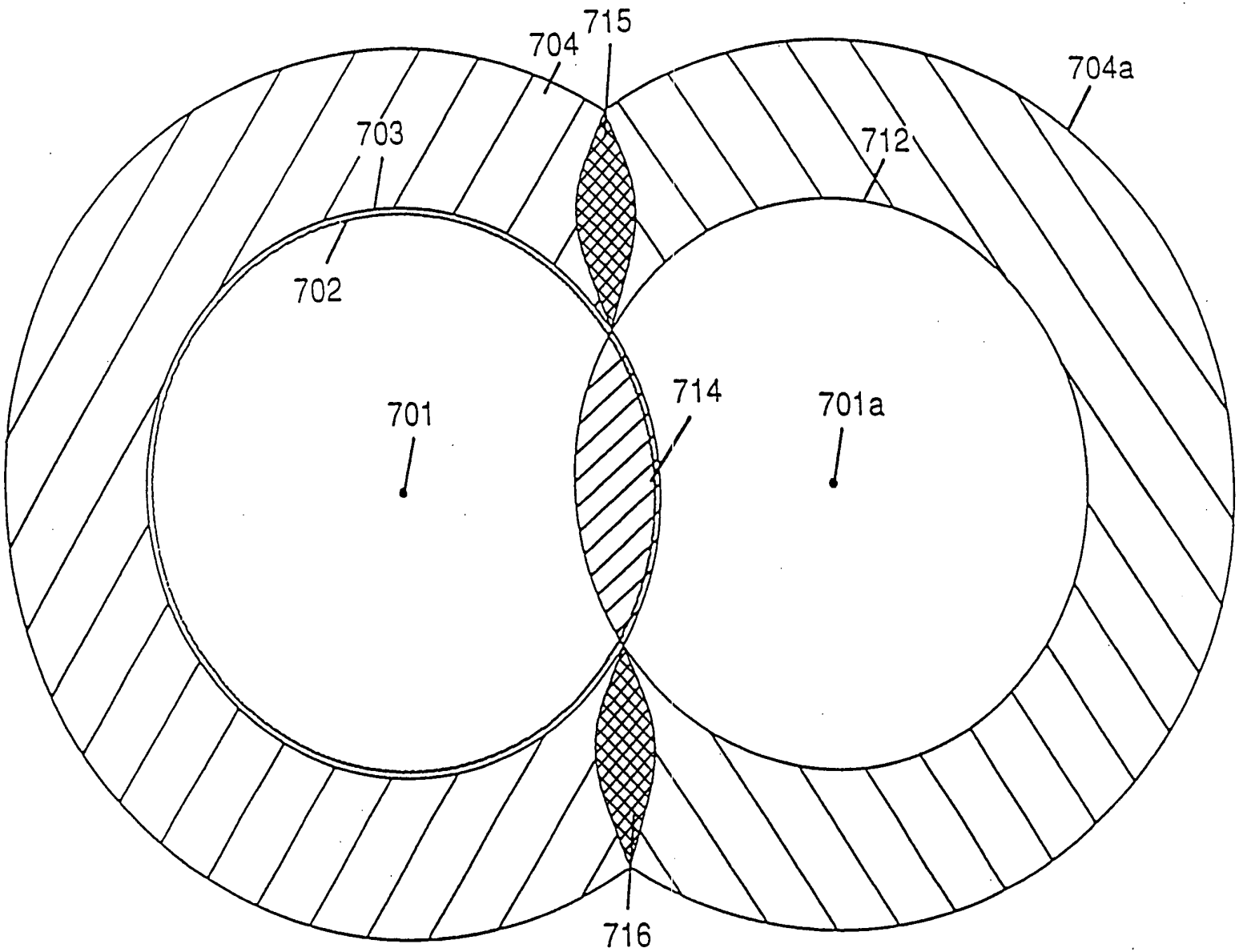


FIG. 57

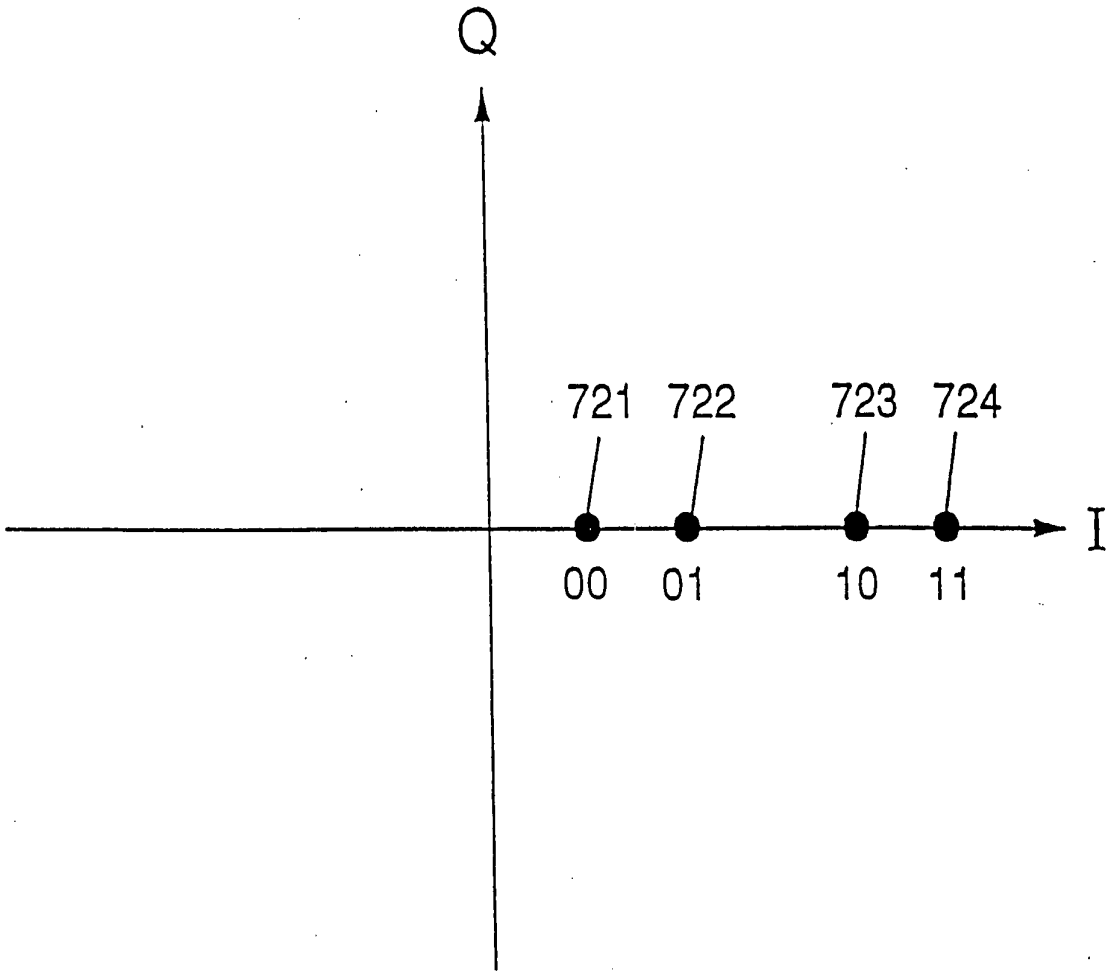


FIG. 58

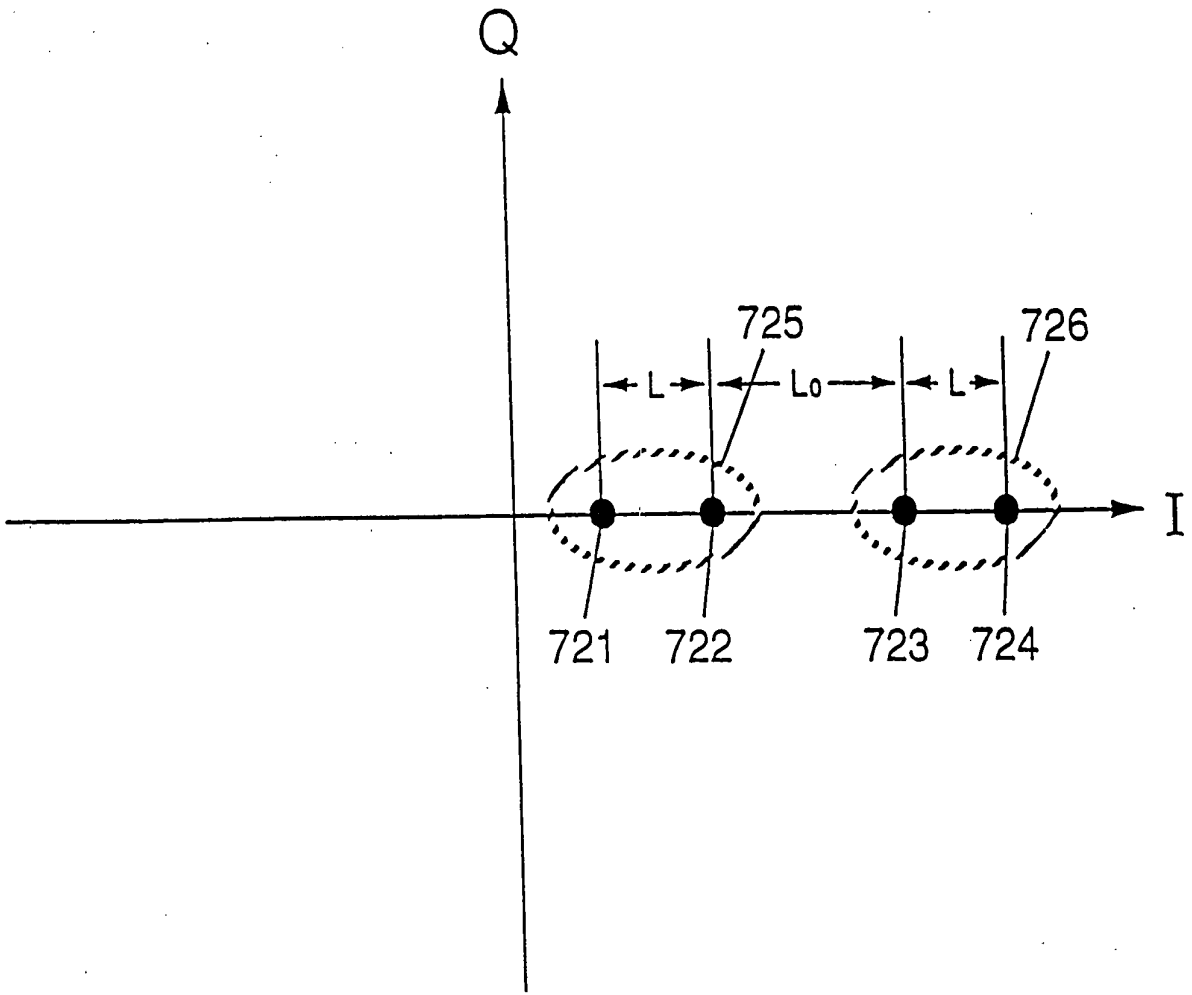


FIG. 59 (a)

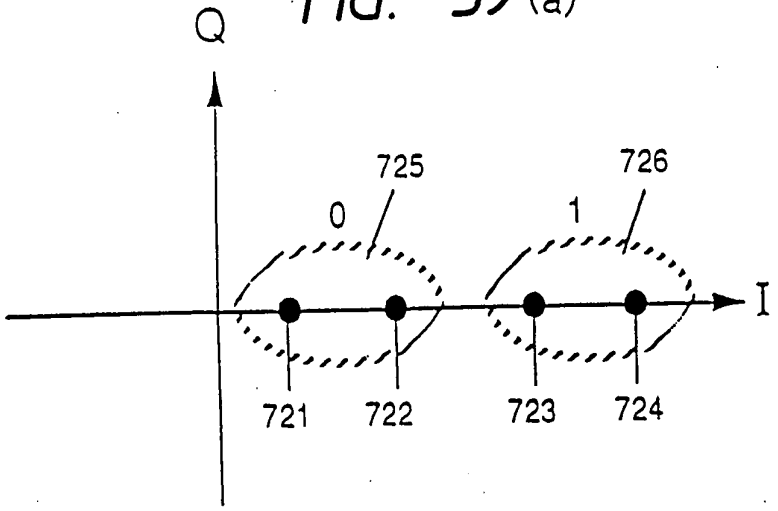


FIG. 59 (b)

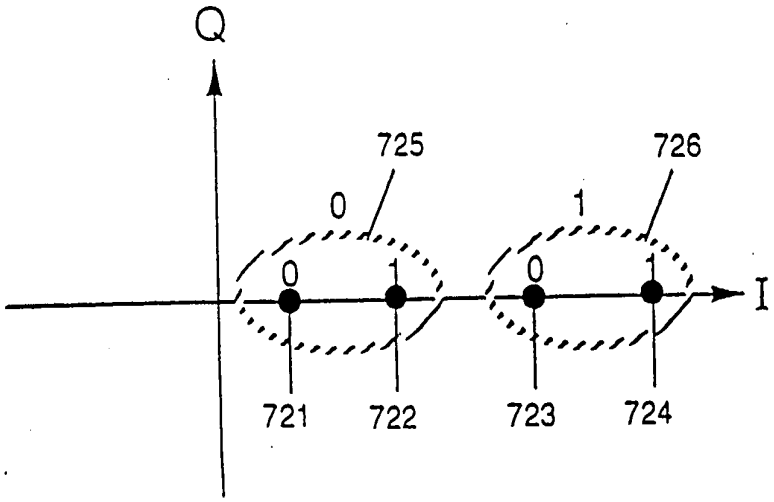


FIG. 59 (c)

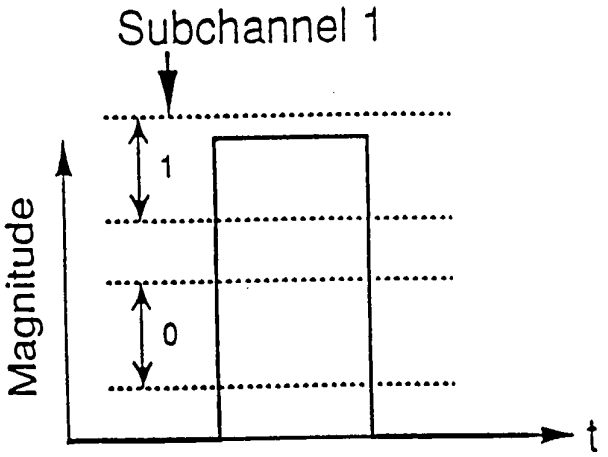


FIG. 59 (d)

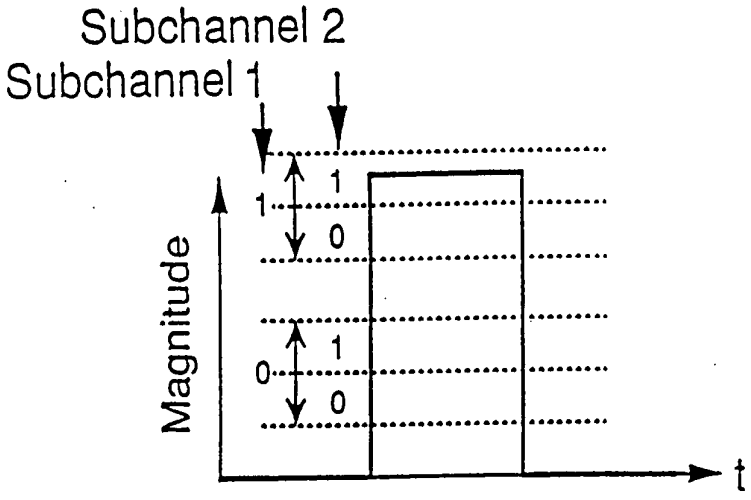


FIG. 60

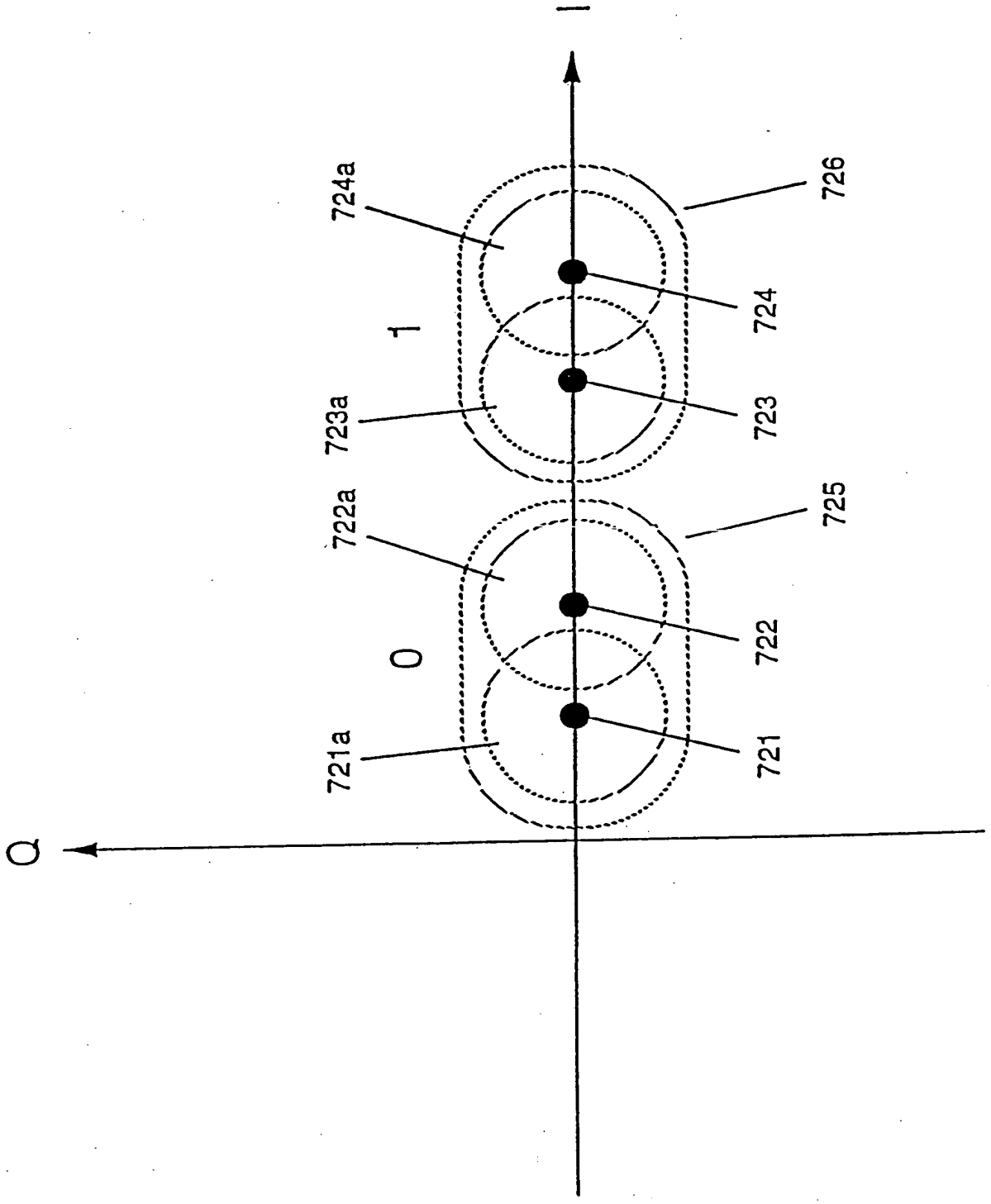


FIG. 61

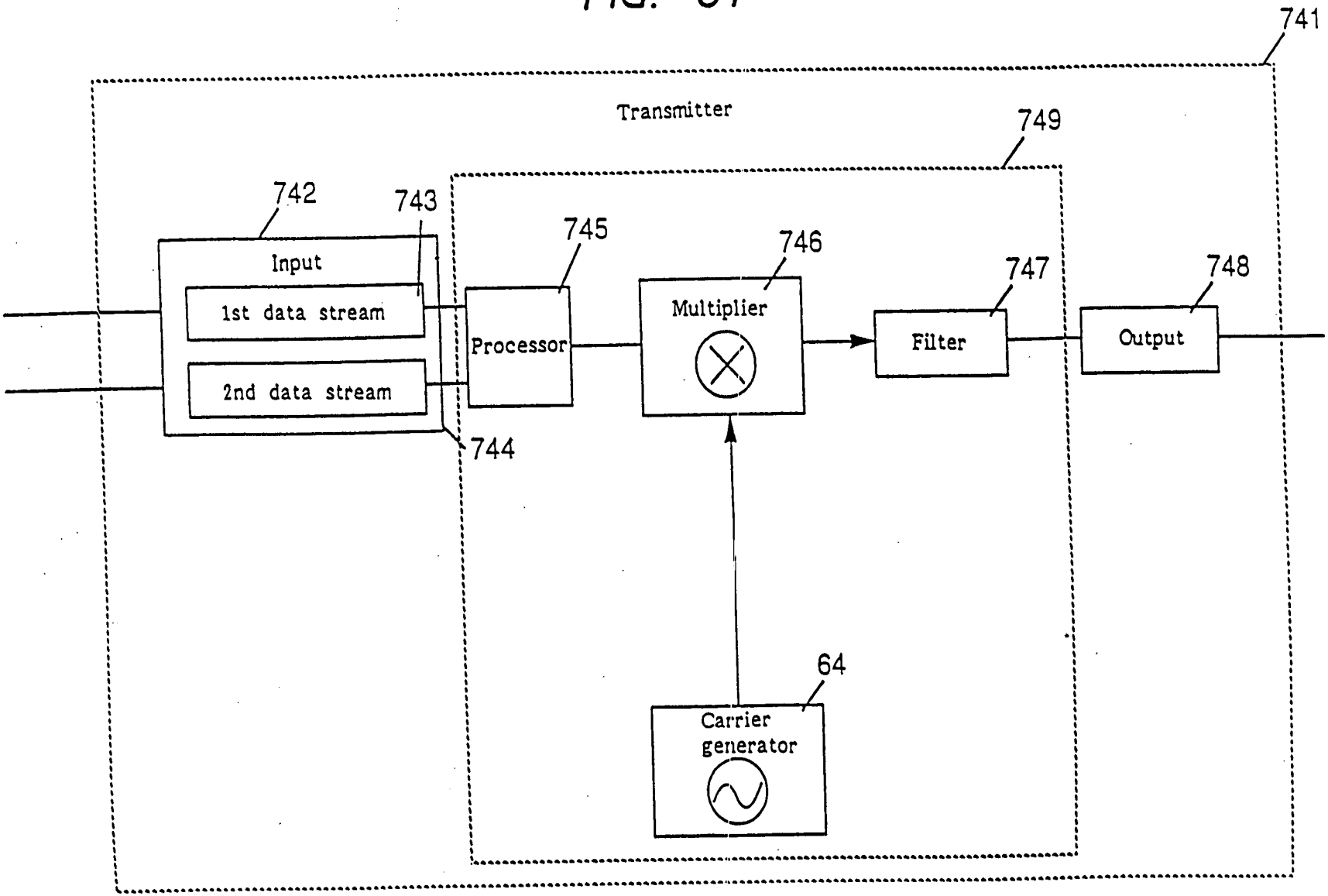

741
Transmitter
749
742
743
745
746
747
748
Input
1st data stream
2nd data stream
Processor
Multiplier
Filter
Output
744
64
Carrier generator

FIG. 62

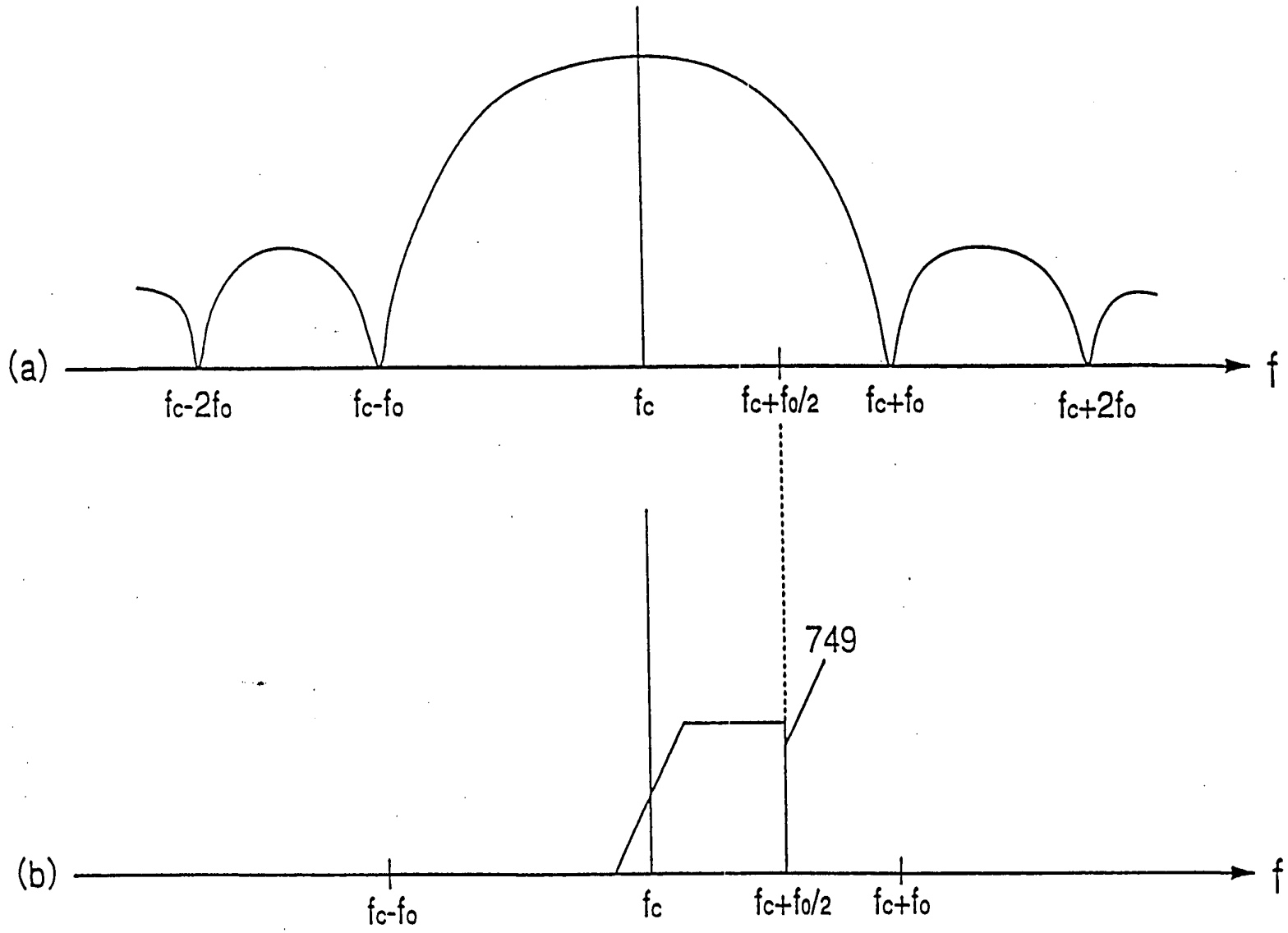


FIG. 63

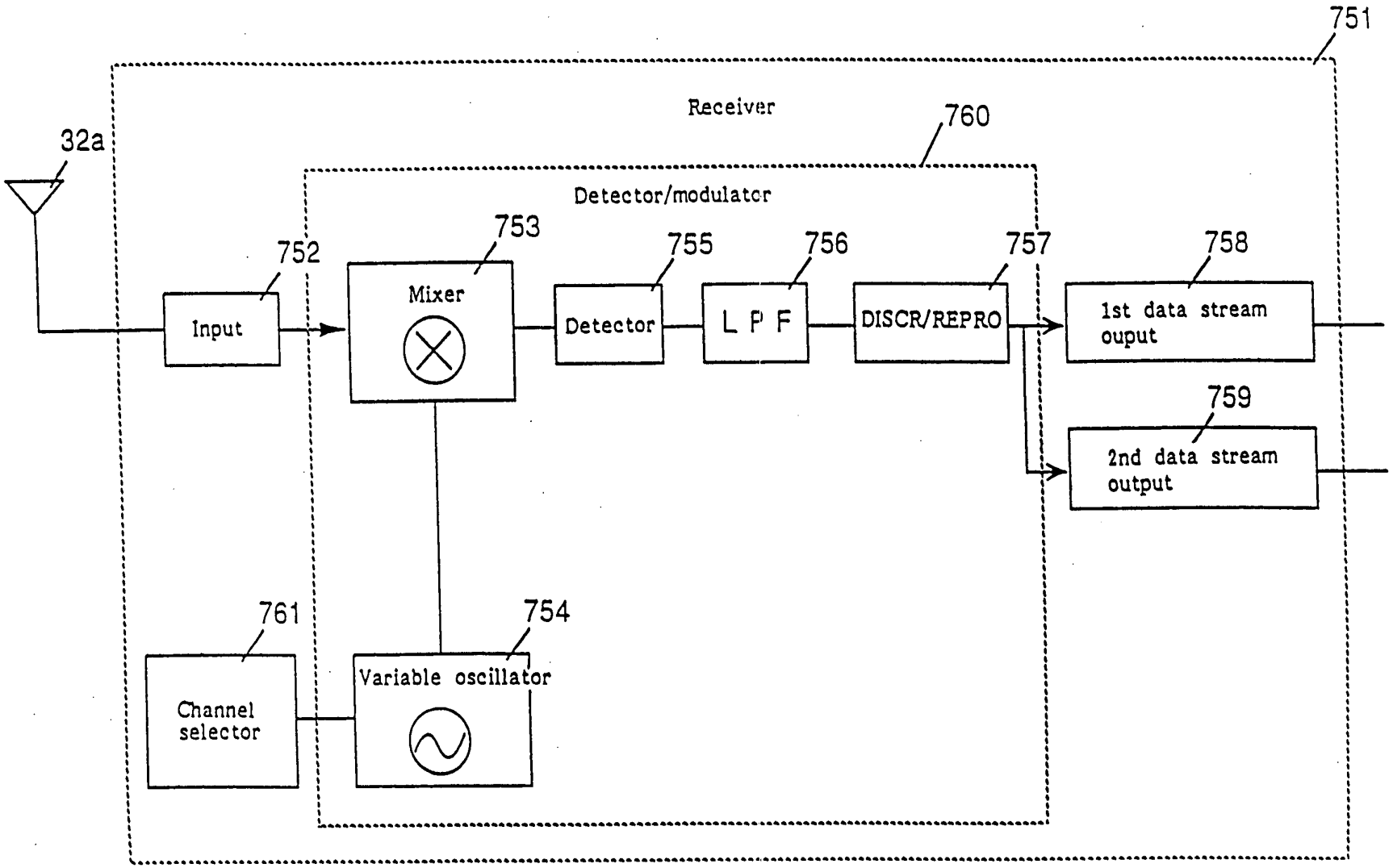

751
Receiver
760
32a
Detector/modulator
753
752
755
756
757
758
Mixer
Input
Detector
L P F
DISCR/REPRO
1st data stream ouput
759
2nd data stream output
761
754
Channel selector
Variable oscillator

FIG. 64

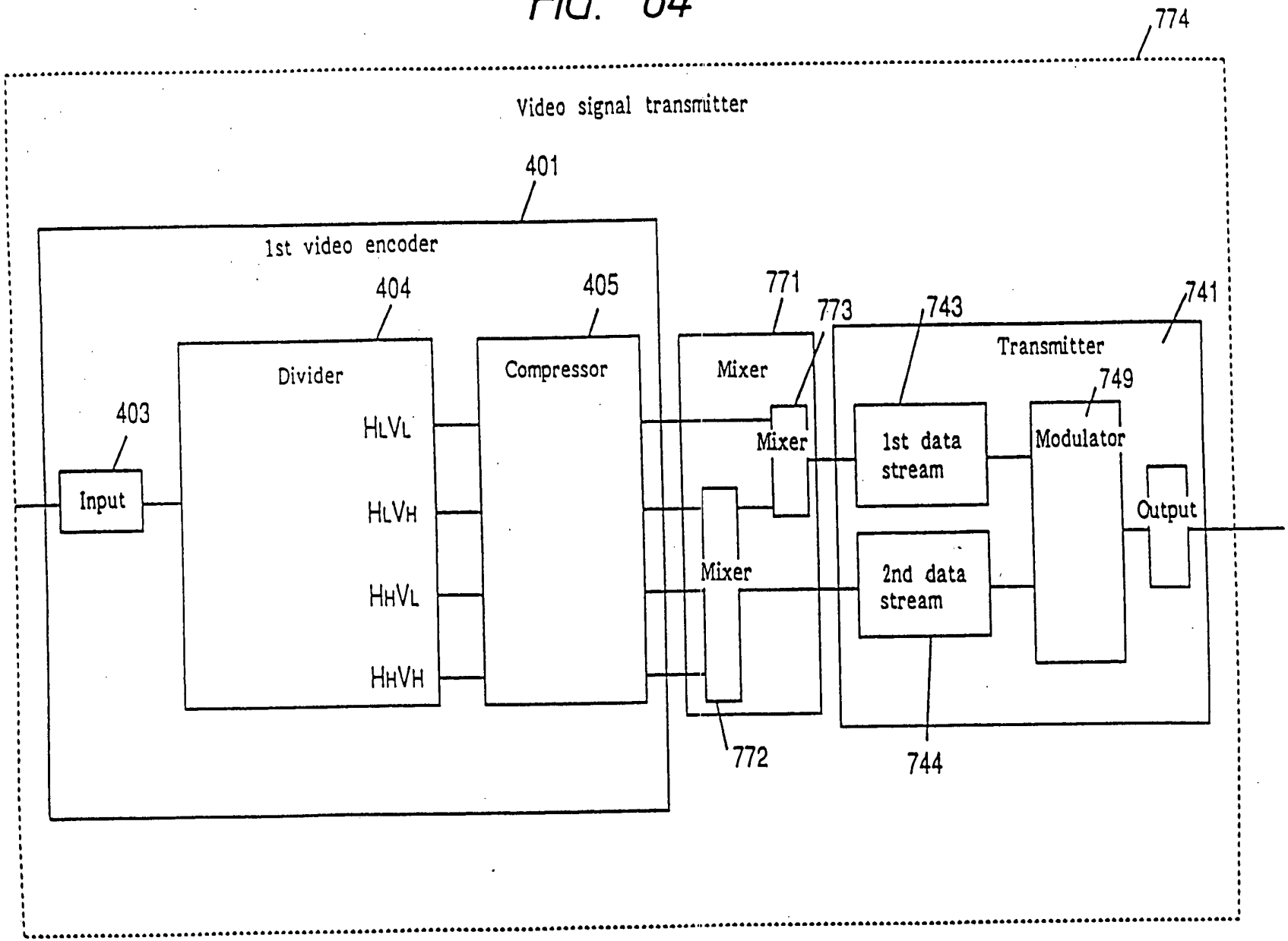

774
Video signal transmitter
401
1st video encoder
404
405
771
773
743
741
Divider
Compressor
Mixer
Transmitter
749
403
HLVL
Mixer
1st data stream
Modulator
Input
HLVH
Output
Mixer
2nd data stream
HHVL
HHVH
772
744

FIG. 65

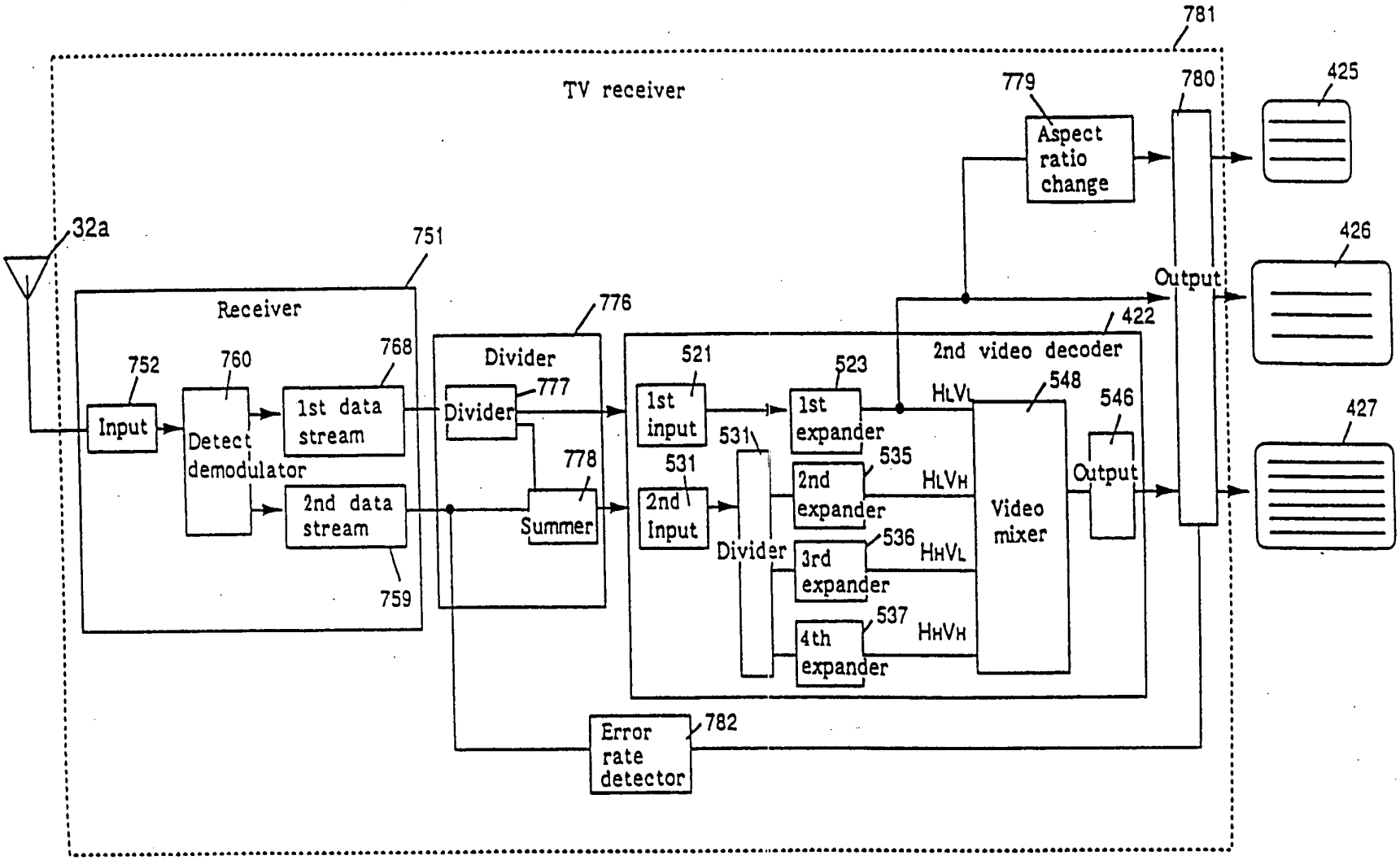

781
TV receiver
779
Aspect ratio change
780
425
426
427
32a
751
Receiver
752
Input
760
Detect demodulator
768
1st data stream
2nd data stream
759
776
Divider
777
Divider
778
Summer
422
2nd video decoder
521
1st input
523
1st expander
531
2nd Input
Divider
535
2nd expander
536
3rd expander
537
4th expander
HLVL
HLVH
HHVL
HHVH
548
Video mixer
546
Output
Output
782
Error rate detector

FIG. 66

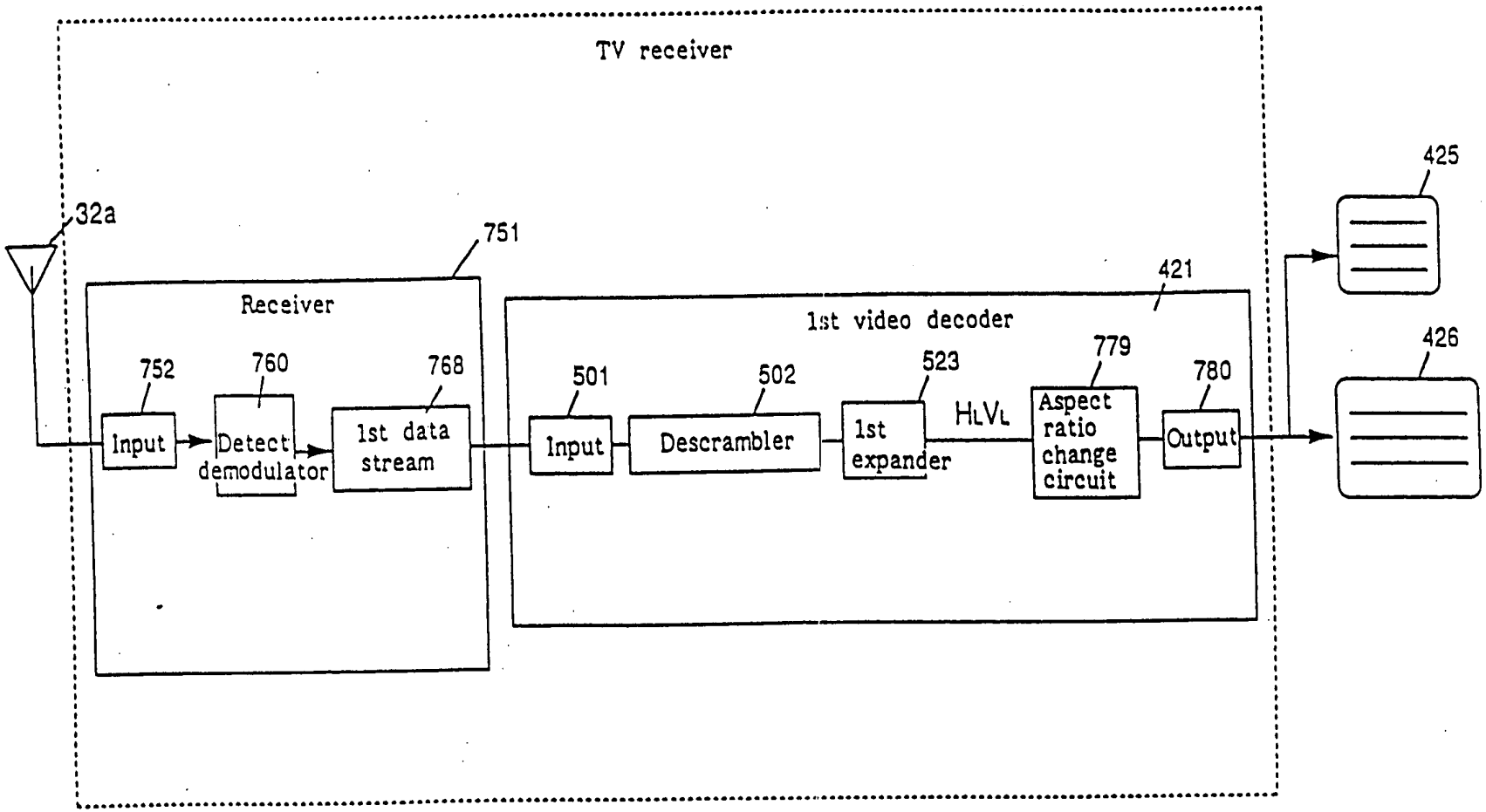

TV receiver
32a
751
Receiver
752
Input
760
Detect demodulator
768
1st data stream
421
1st video decoder
501
Input
502
Descrambler
523
1st expander
HLVL
779
Aspect ratio change circuit
780
Output
425
426

FIG. 67

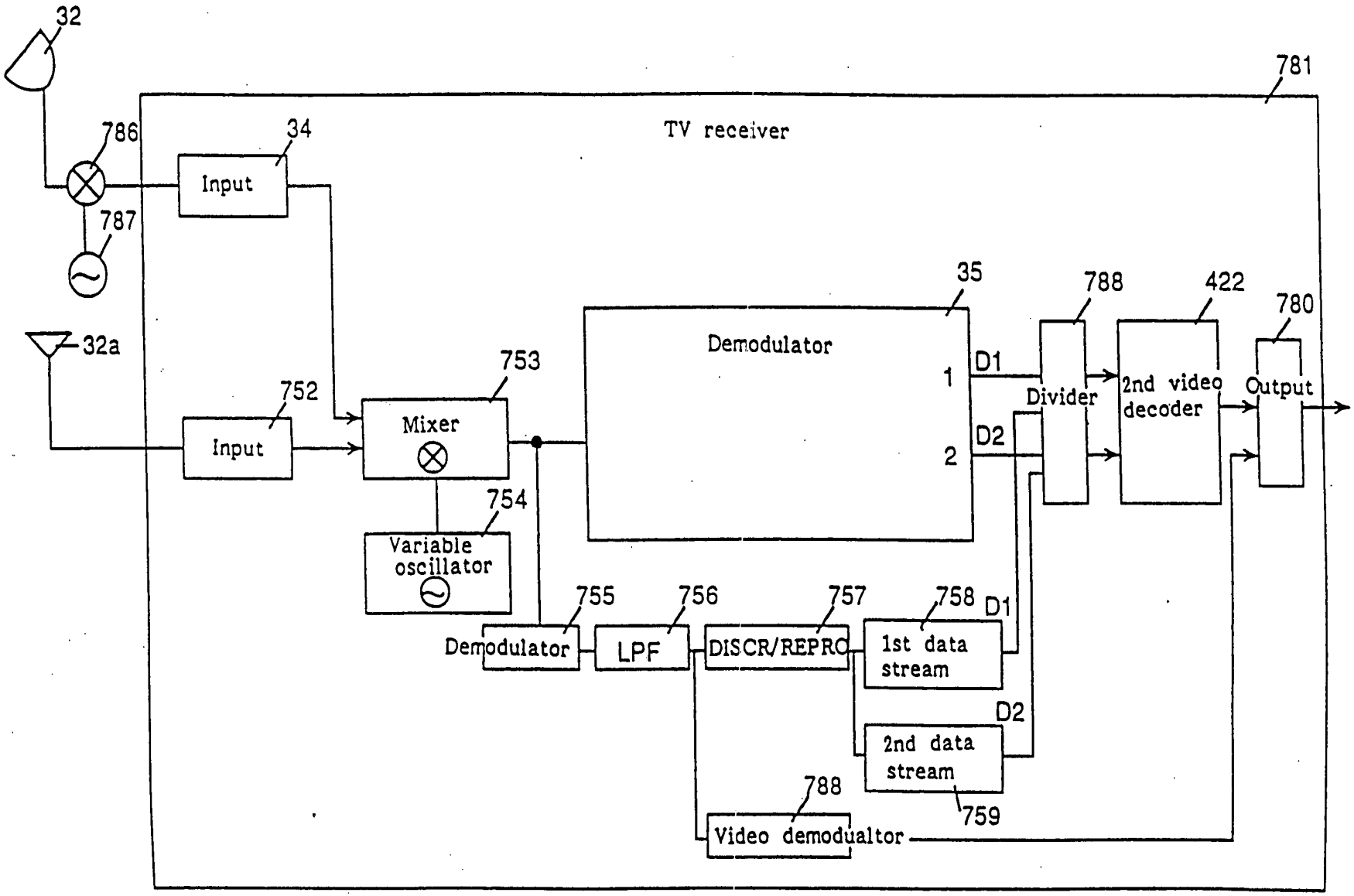

32
781
TV receiver
786
34
Input
787
35
788
422
780
Demodulator
32a
753
D1
1
752
Input
Mixer
Divider
2nd video decoder
Output
D2
2
754
Variable oscillator
755
756
757
758
D1
Demodulator
LPF
DISCR/REPRO
1st data stream
D2
2nd data stream
759
788
Video demodualtor

FIG. 68

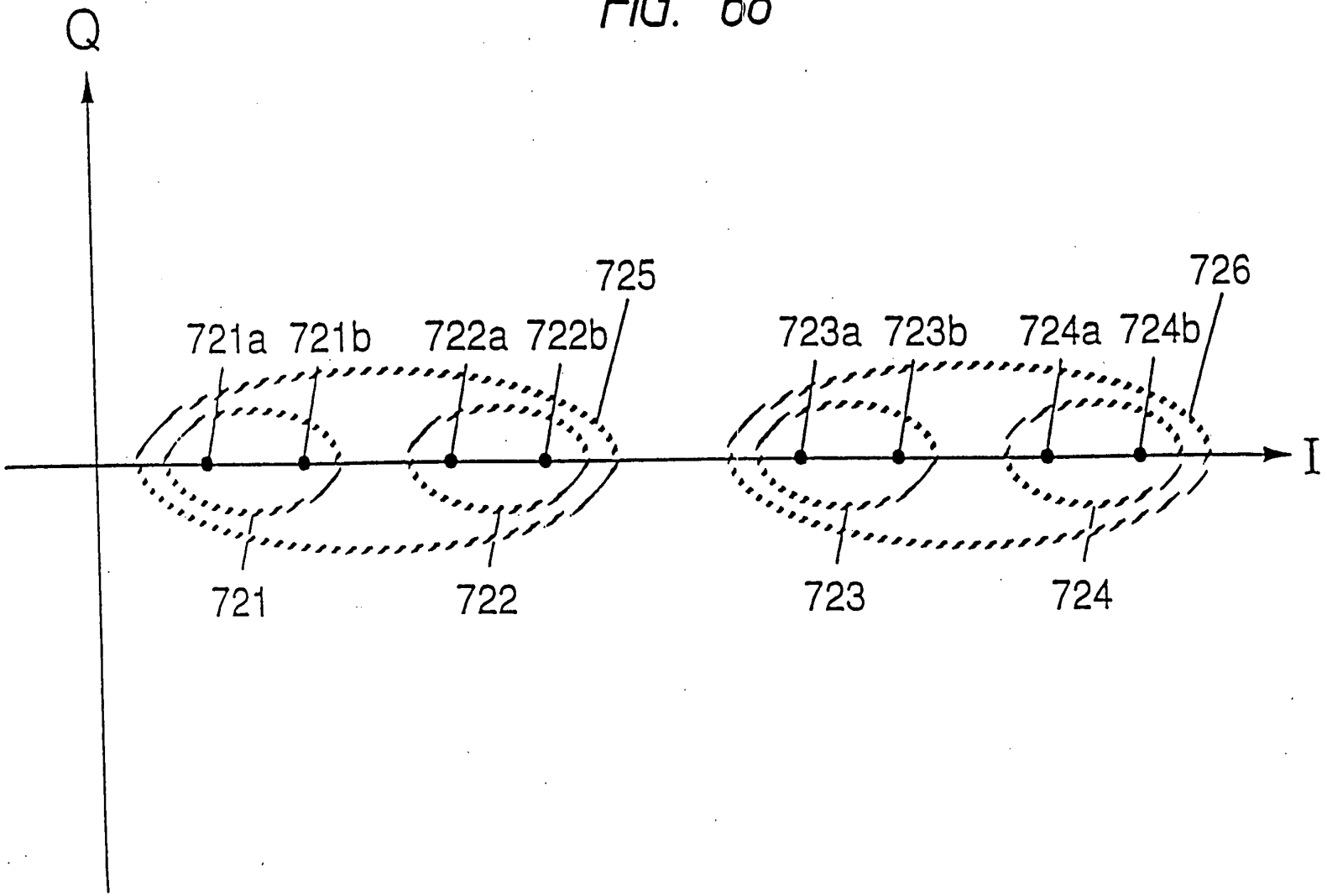

Q
I
721a
721b
722a
722b
725
723a
723b
724a
724b
726
721
722
723
724

FIG. 69

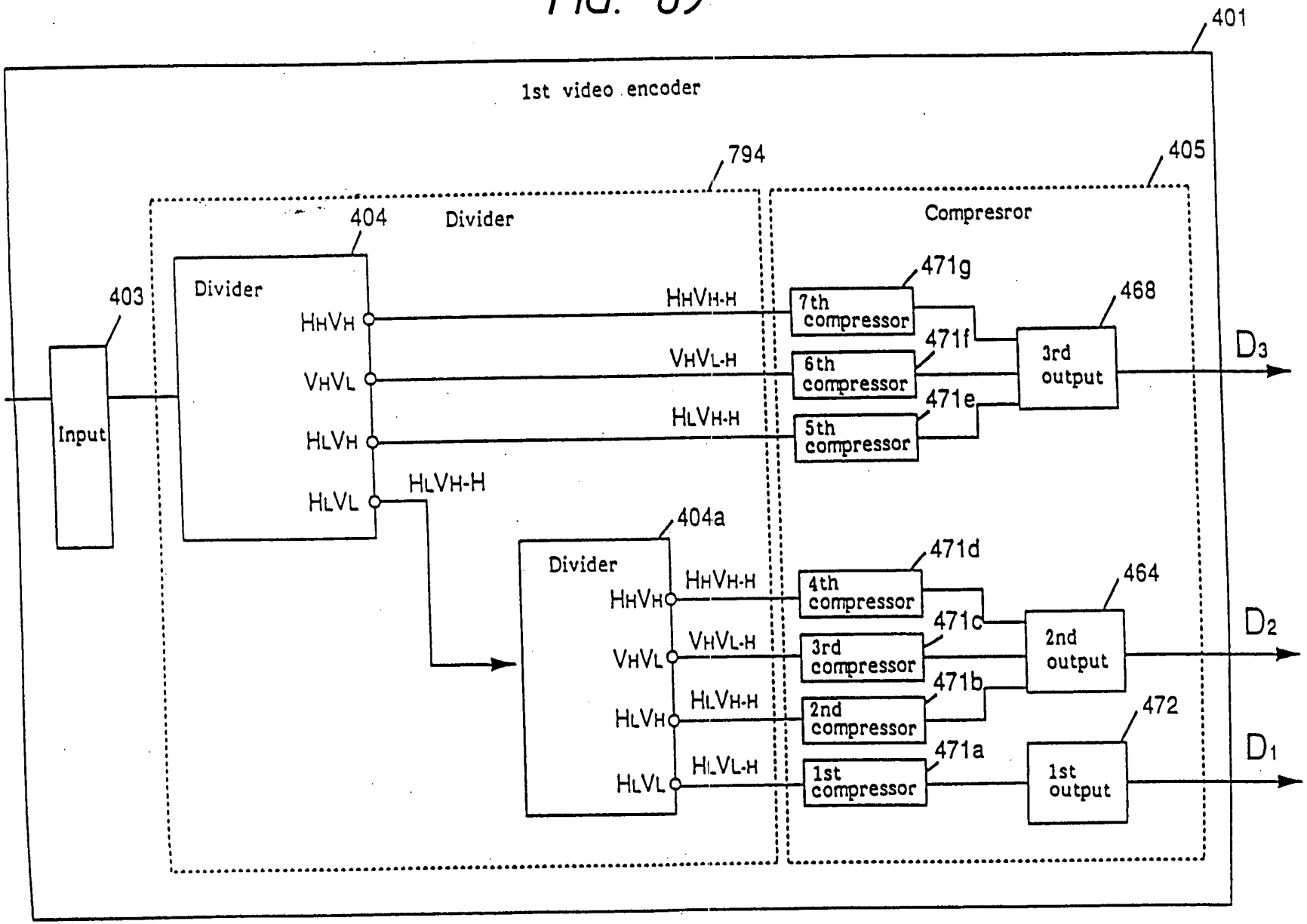

401
1st video encoder
794
405
404
Divider
Compresror
Divider
403
Input
HHVH
VHVL
HLVH
HLVL
HLVH-H
HHVH-H
VHVL-H
HLVH-H
HLVL-H
471g
7th compressor
471f
6th compressor
471e
5th compressor
468
3rd output
D3
404a
Divider
HHVH
VHVL
HLVH
HLVL
HHVH-H
VHVL-H
HLVH-H
HLVL-H
471d
4th compressor
471c
3rd compressor
471b
2nd compressor
471a
1st compressor
464
2nd output
D2
472
1st output
D1

FIG. 70

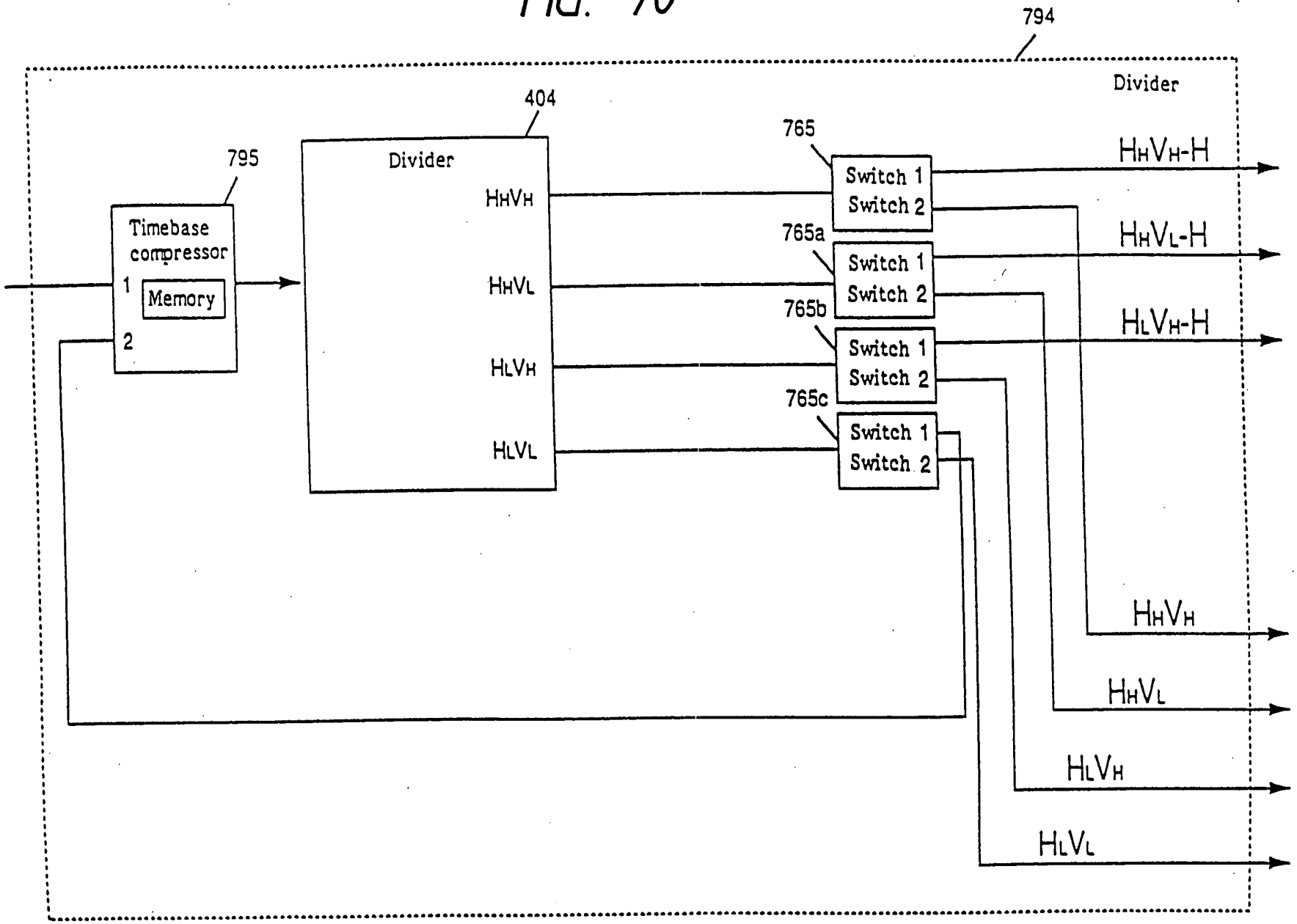

794
Divider
404
Divider
795
Timebase compressor
1
Memory
2
HHVH
HHVL
HLVH
HLVL
765
Switch 1
Switch 2
765a
Switch 1
Switch 2
765b
Switch 1
Switch 2
765c
Switch 1
Switch 2
HHVH-H
HHVL-H
HLVH-H
HHVH
HHVL
HLVH
HLVL

FIG. 71

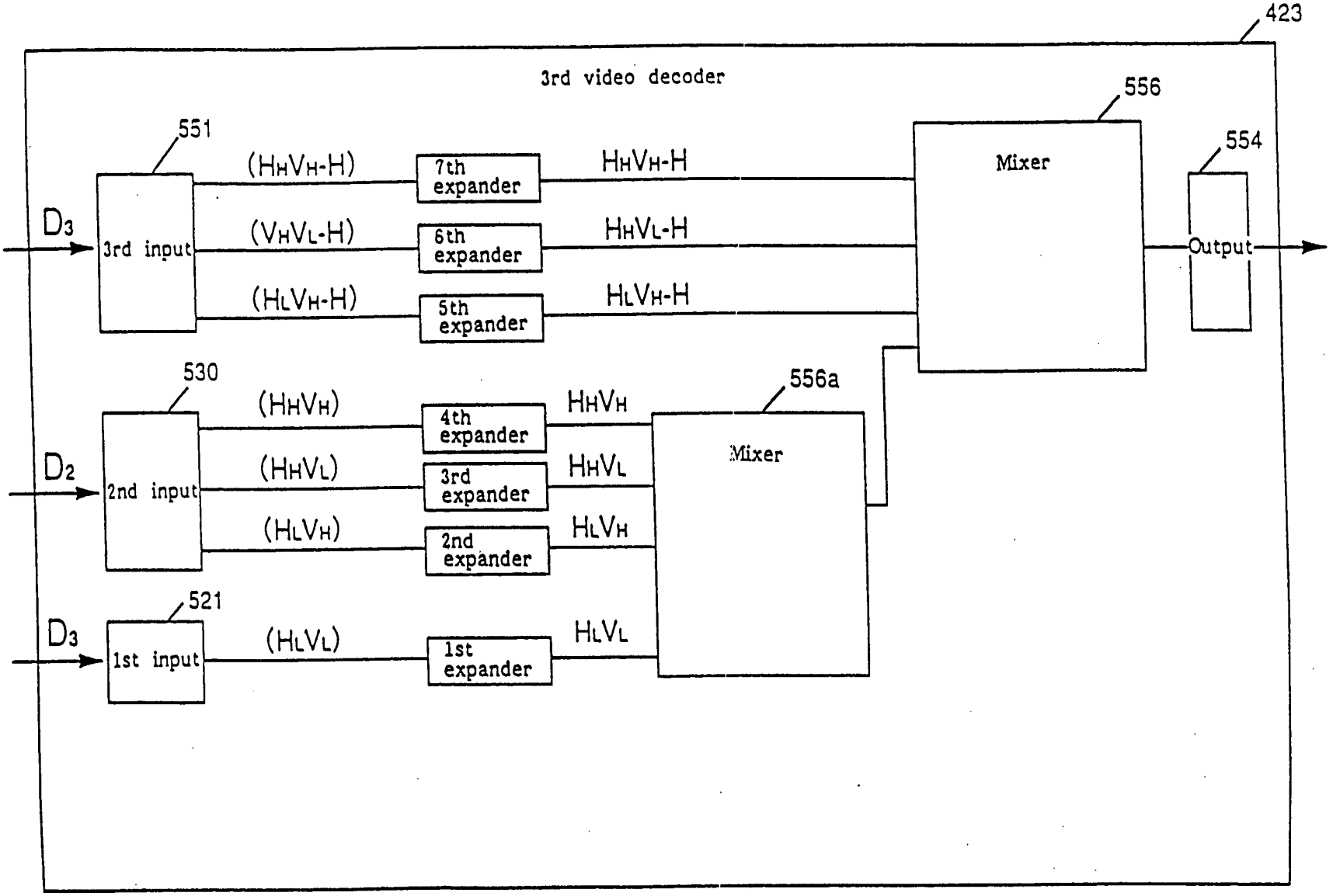

423
3rd video decoder
556
551
554
(HHVH-H)
7th expander
HHVH-H
Mixer
D3
3rd input
(VHVL-H)
6th expander
HHVL-H
Output
(HLVH-H)
5th expander
HLVH-H
530
556a
(HHVH)
4th expander
HHVH
D2
2nd input
(HHVL)
3rd expander
HHVL
Mixer
(HLVH)
2nd expander
HLVH
521
D3
1st input
(HLVL)
1st expander
HLVL

FIG. 72

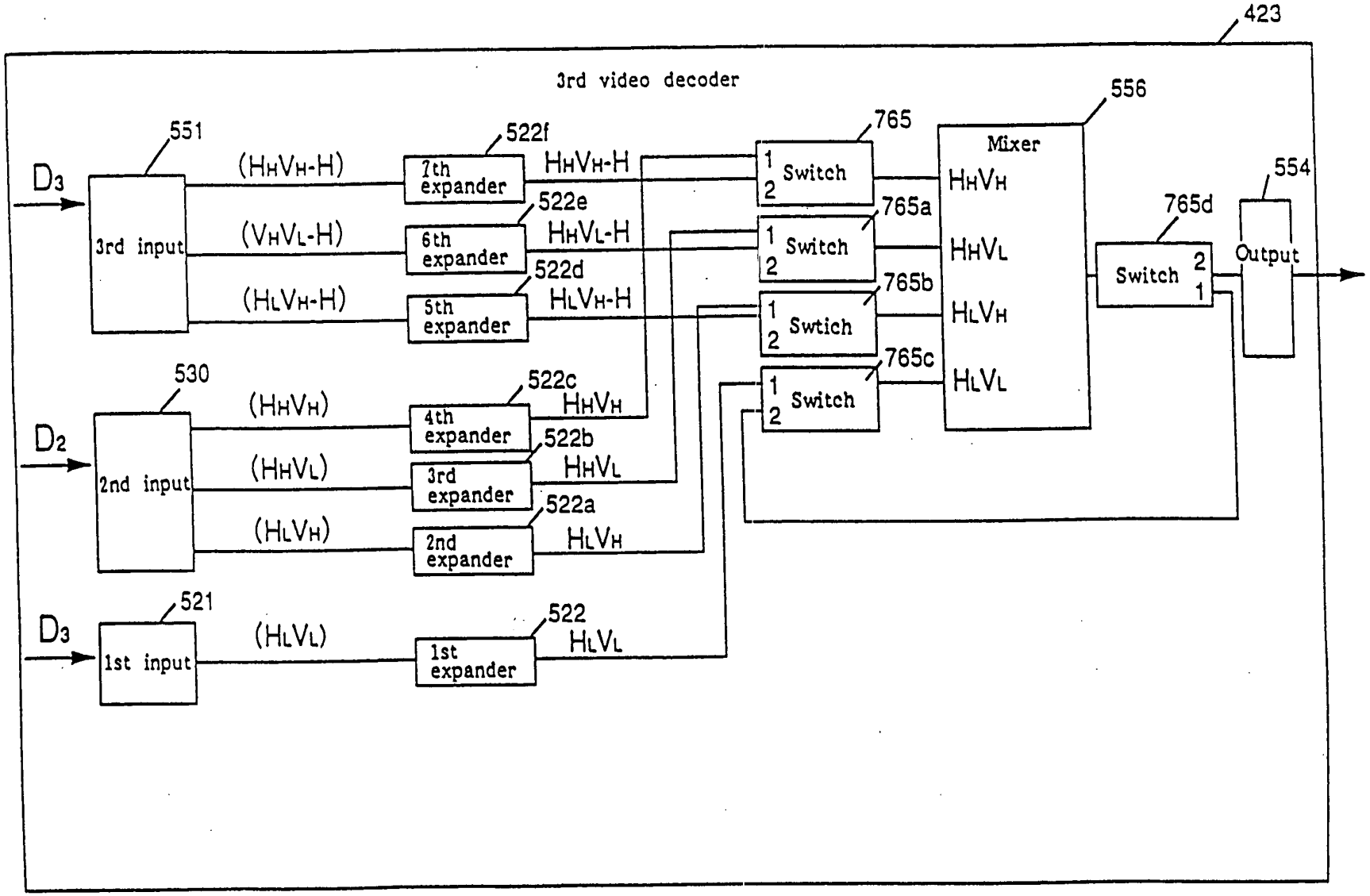

423
3rd video decoder
556
Mixer
765
551
522f
554
D3
(HHVH-H)
7th expander
HHVH-H
1 Switch 2
HHVH
3rd input
(VHVL-H)
522e
6th expander
HHVL-H
765a
HHVL
765d
Output
(HLVH-H)
522d
5th expander
HLVH-H
765b
HLVH
Switch 2 1
530
522c
765c
D2
(HHVH)
4th expander
HHVH
HLVL
2nd input
(HHVL)
522b
3rd expander
HHVL
(HLVH)
522a
2nd expander
HLVH
521
522
D3
(HLVL)
1st input
1st expander
HLVL

FIG. 73

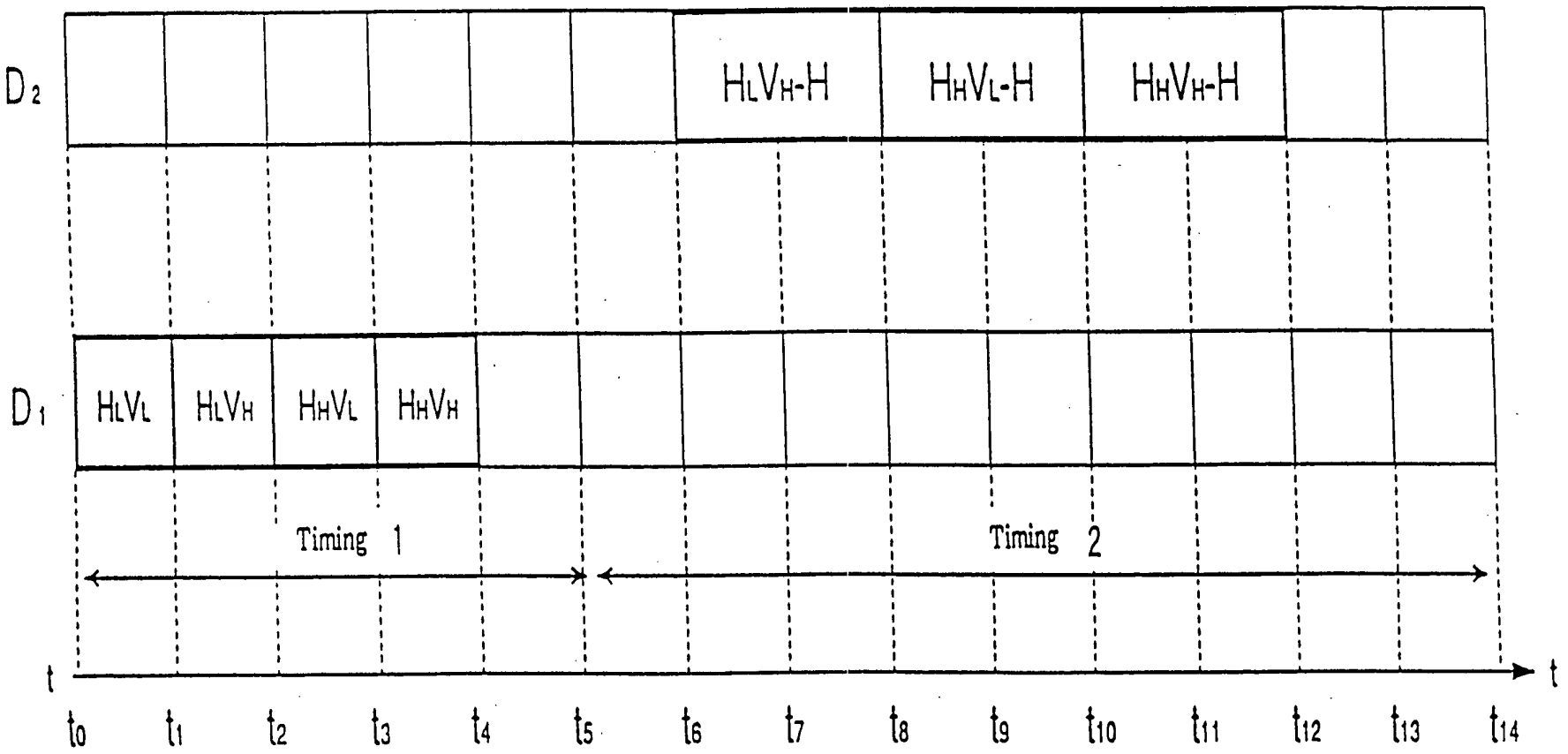

D2
HLVH-H
HHVL-H
HHVH-H
D1
HLVL
HLVH
HHVL
HHVH
Timing 1
Timing 2
t
t
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14

FIG. 74

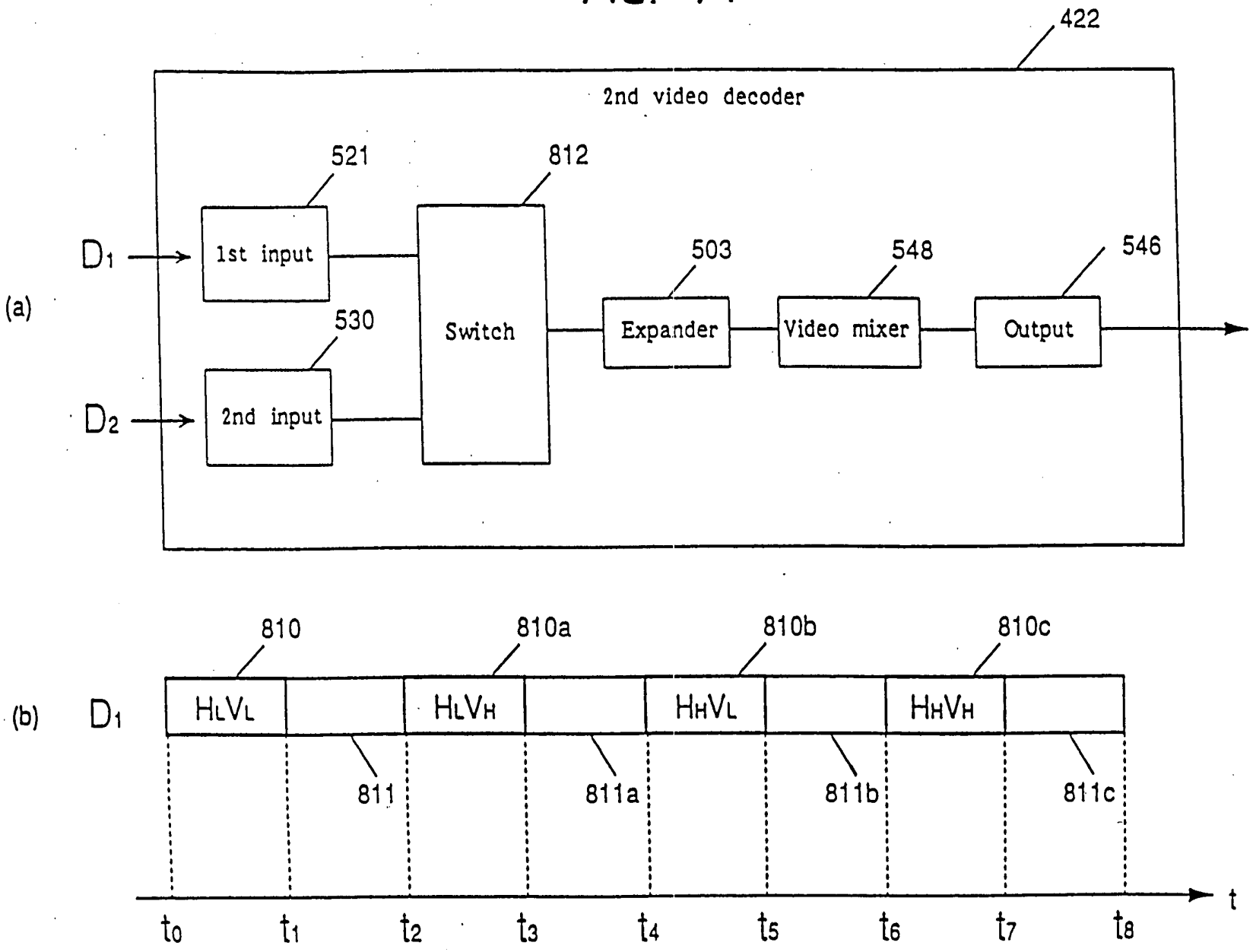

422
2nd video decoder
521
812
D1
1st input
Switch
503
548
546
(a)
530
Expander
Video mixer
Output
D2
2nd input
810
810a
810b
810c
(b)
D1
HLVL
HLVH
HHVL
HHVH
811
811a
811b
811c
t
t0
t1
t2
t3
t4
t5
t6
t7
t8

FIG. 75

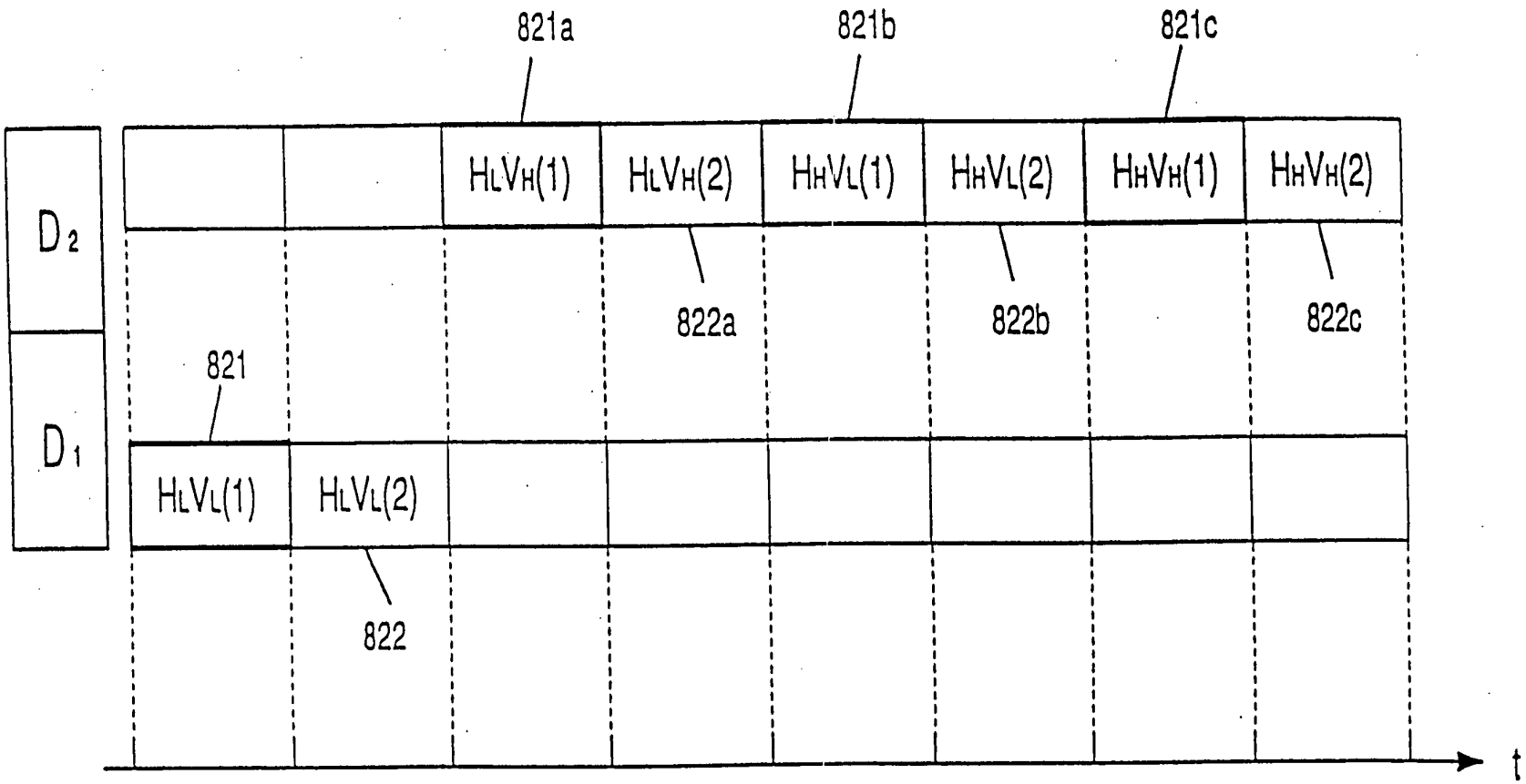

821a
821b
821c
D2
D1
HLVH(1)
HLVH(2)
HHVL(1)
HHVL(2)
HHVH(1)
HHVH(2)
822a
822b
822c
821
HLVL(1)
HLVL(2)
822
t

FIG. 76

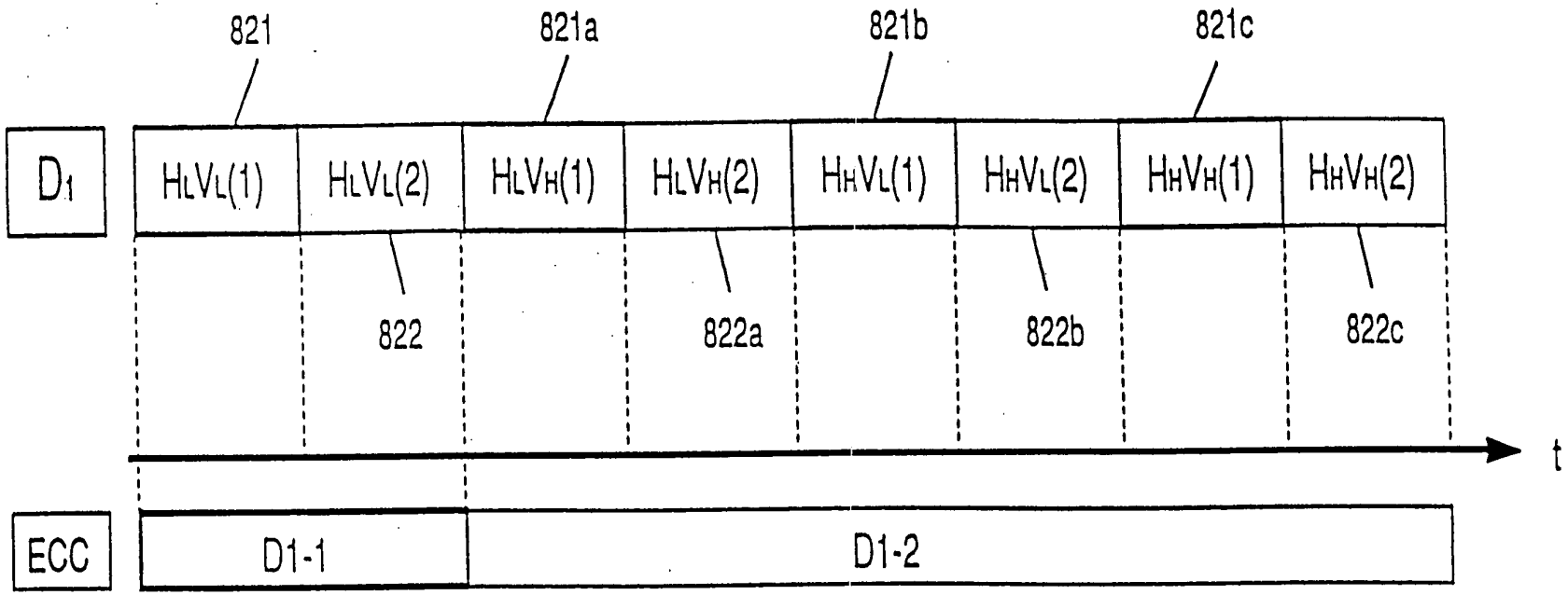

821
821a
821b
821c
D1
HLVL(1)
HLVL(2)
HLVH(1)
HLVH(2)
HHVL(1)
HHVL(2)
HHVH(1)
HHVH(2)
822
822a
822b
822c
t
ECC
D1-1
D1-2

FIG. 77

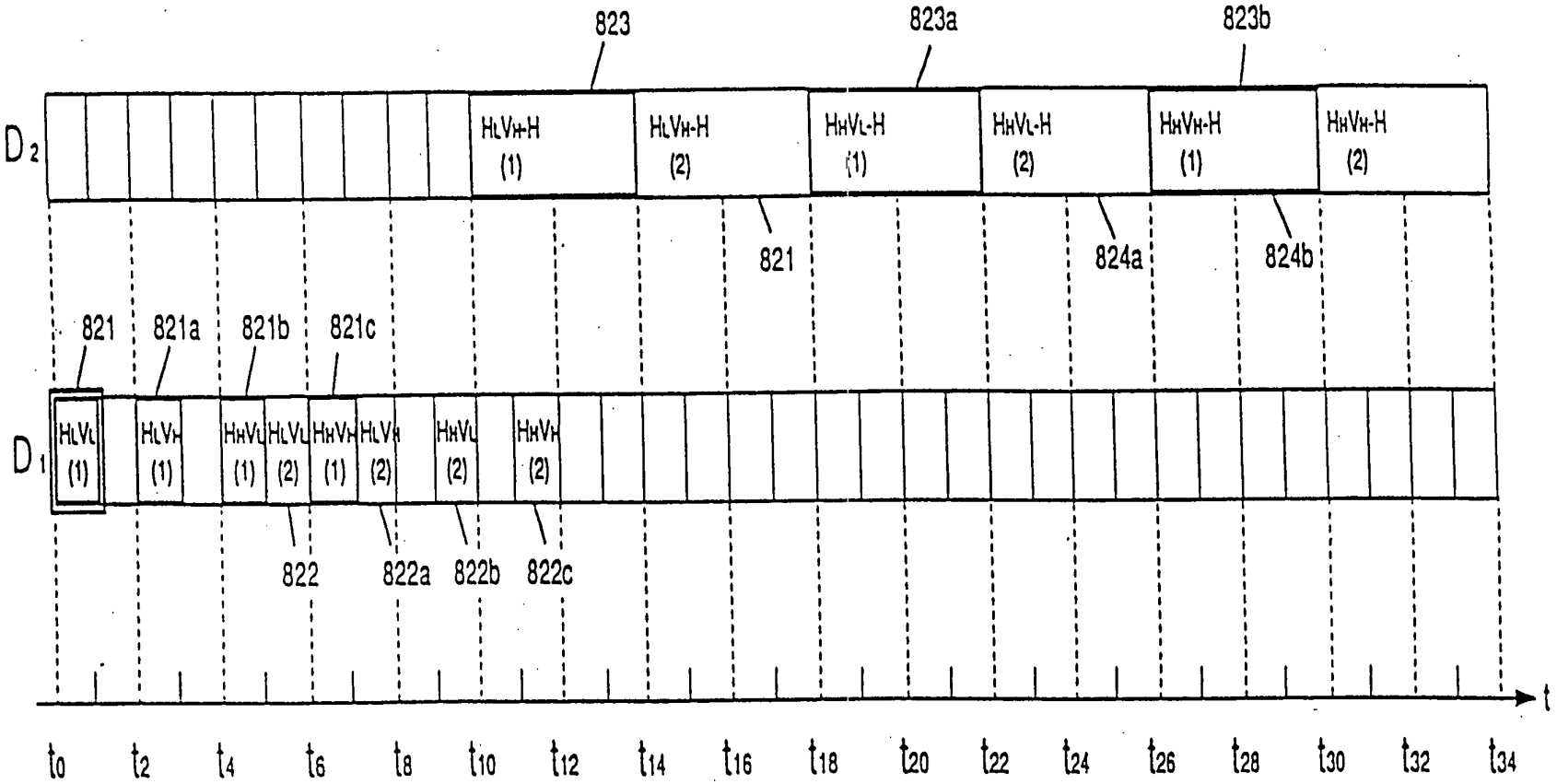

823
823a
823b
D2
HLVH-H (1)
HLVH-H (2)
HHVL-H (1)
HHVL-H (2)
HHVH-H (1)
HHVH-H (2)
821
824a
824b
821
821a
821b
821c
D1
HLVL (1)
HLVH (1)
HHVL (1)
HLVL (2)
HHVH (1)
HLVH (2)
HHVL (2)
HHVH (2)
822
822a
822b
822c
t
t0
t2
t4
t6
t8
t10
t12
t14
t16
t18
t20
t22
t24
t26
t28
t30
t32
t34

FIG. 78

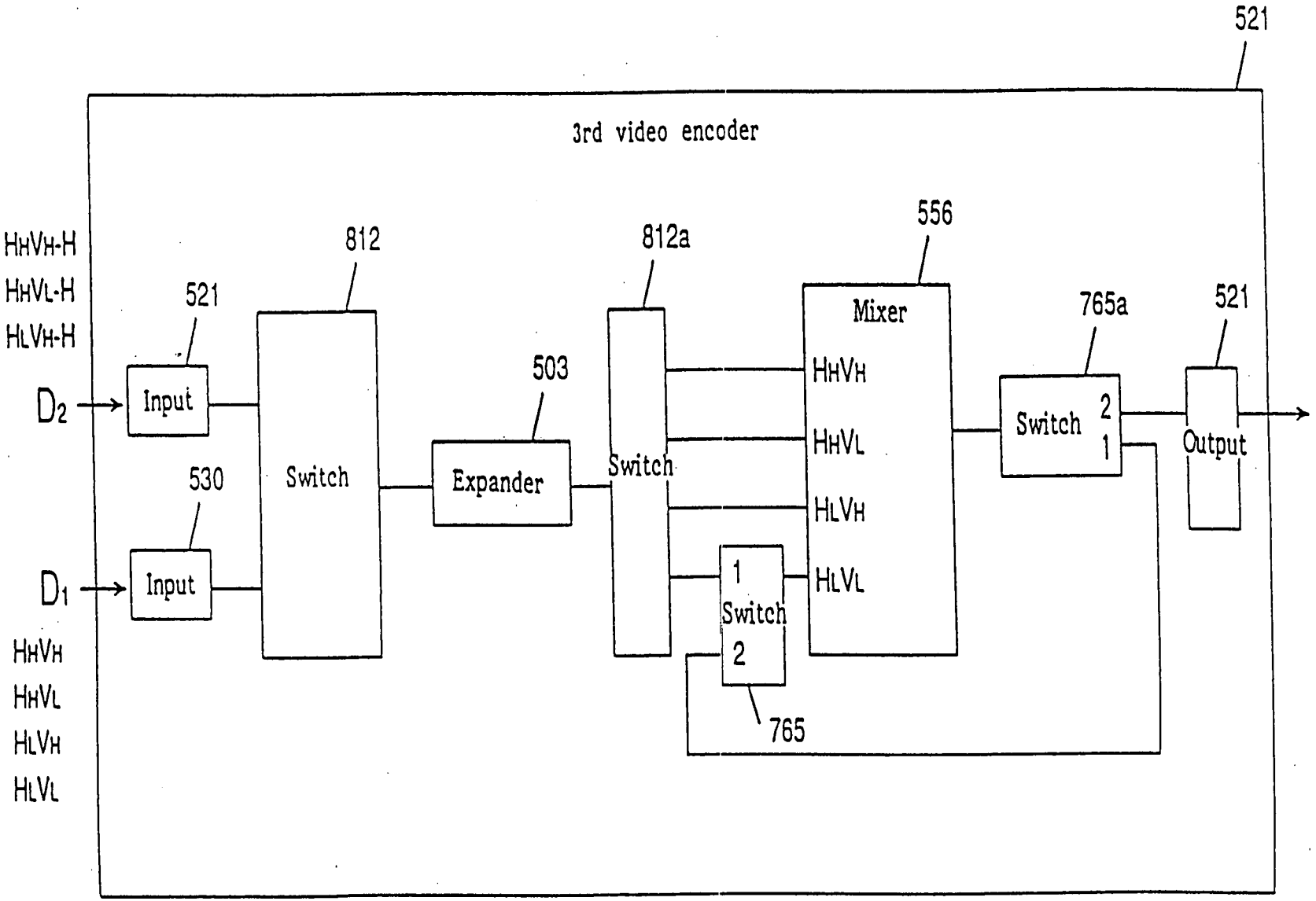

521
3rd video encoder
HHVH-H
HHVL-H
HLVH-H
812
812a
556
521
Mixer
765a
521
503
D2
Input
Switch
Expander
Switch
HHVH
HHVL
HLVH
HLVL
Switch
2
1
Output
530
D1
Input
1
Switch
2
765
HHVH
HHVL
HLVH
HLVL

FIG. 79

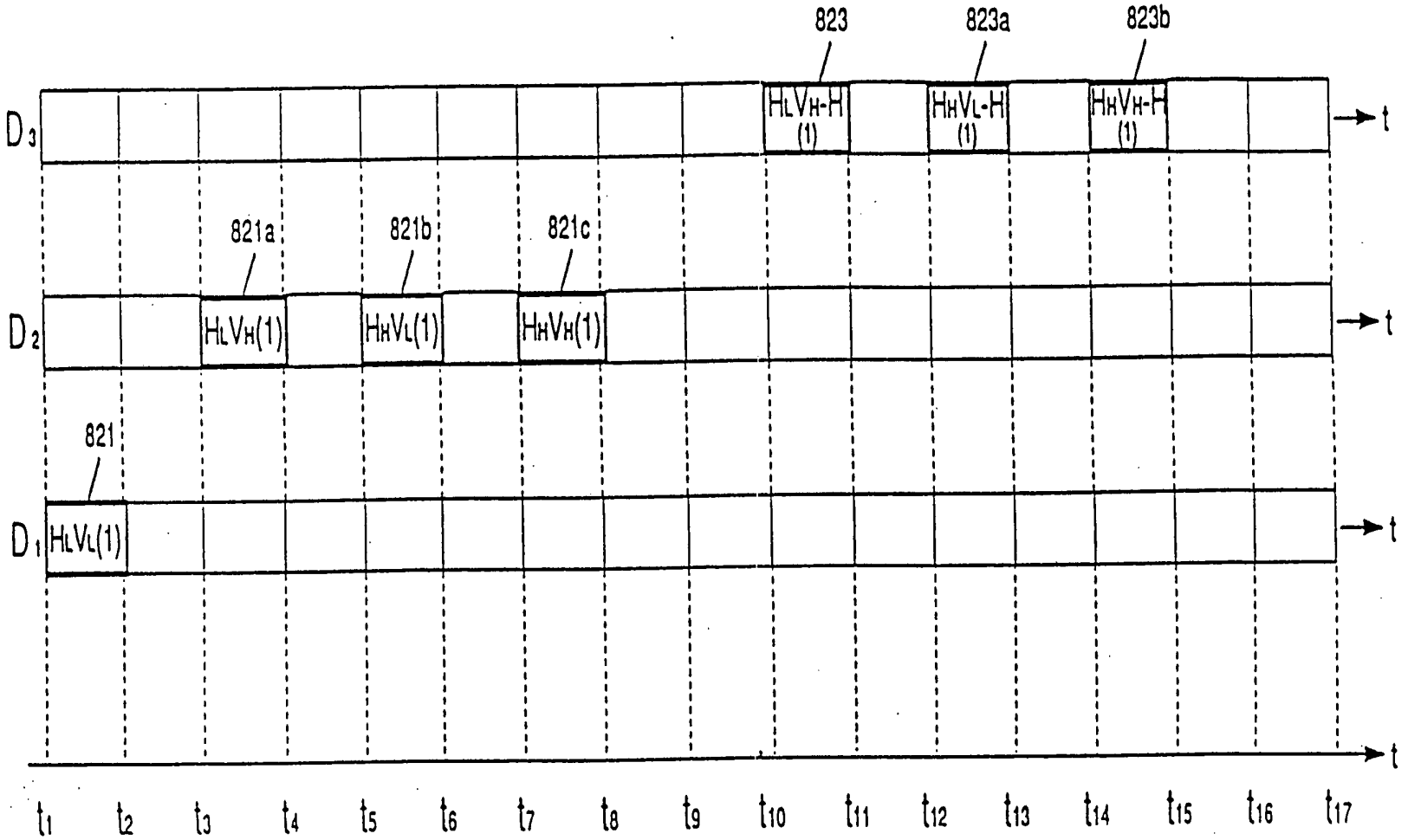

823
823a
823b
D3
D2
D1
HLVH-H (1)
HHVL-H (1)
HHVH-H (1)
821a
821b
821c
HLVH(1)
HHVL(1)
HHVH(1)
821
HLVL(1)
t
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
t16
t17

FIG. 80

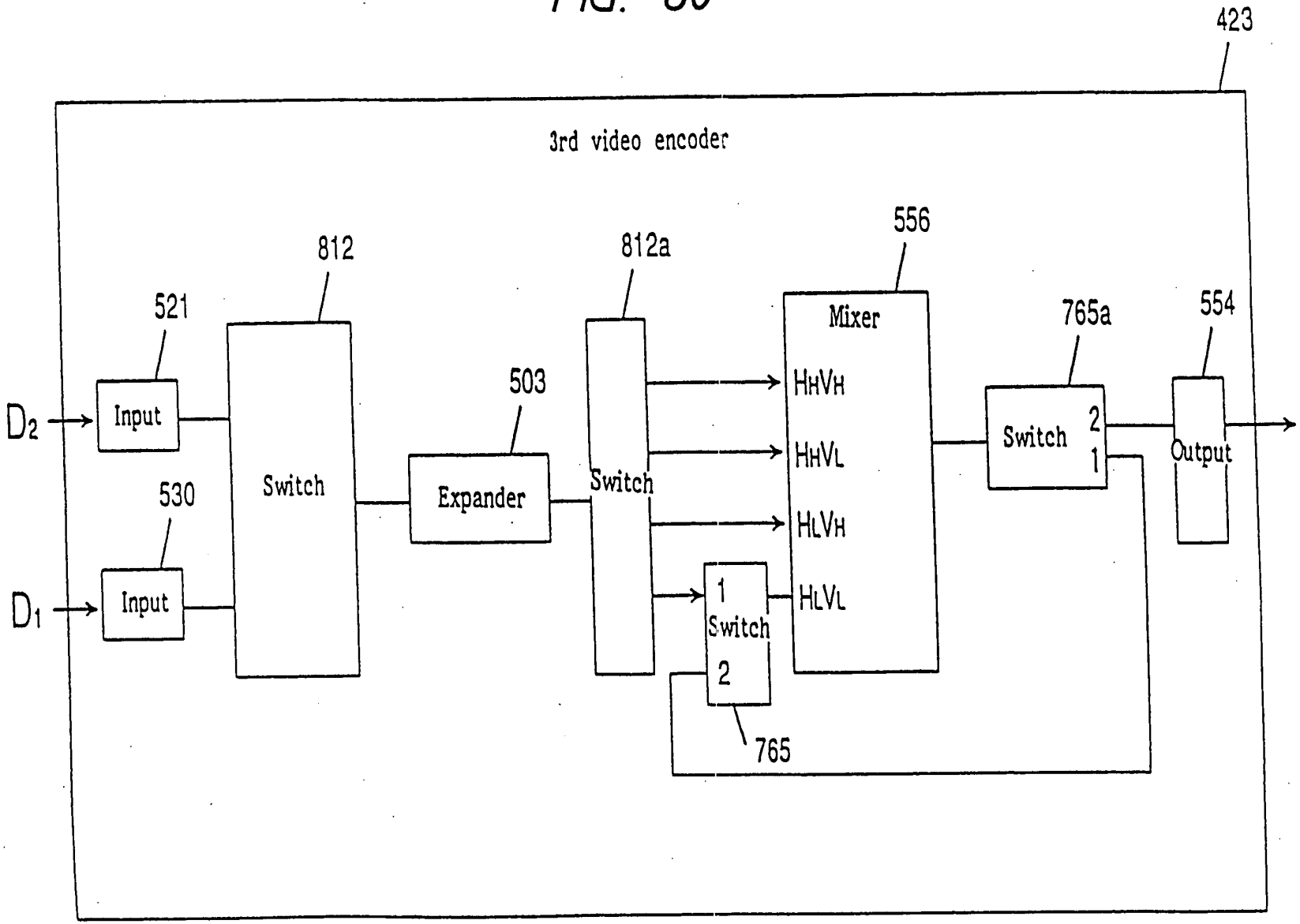

423
3rd video encoder
812
812a
556
521
Mixer
765a
554
503
D2
Input
Switch
Switch
Expander
HHVH
HHVL
HLVH
HLVL
Switch
2
1
Output
530
D1
Input
1
Switch
2
765

FIG. 81

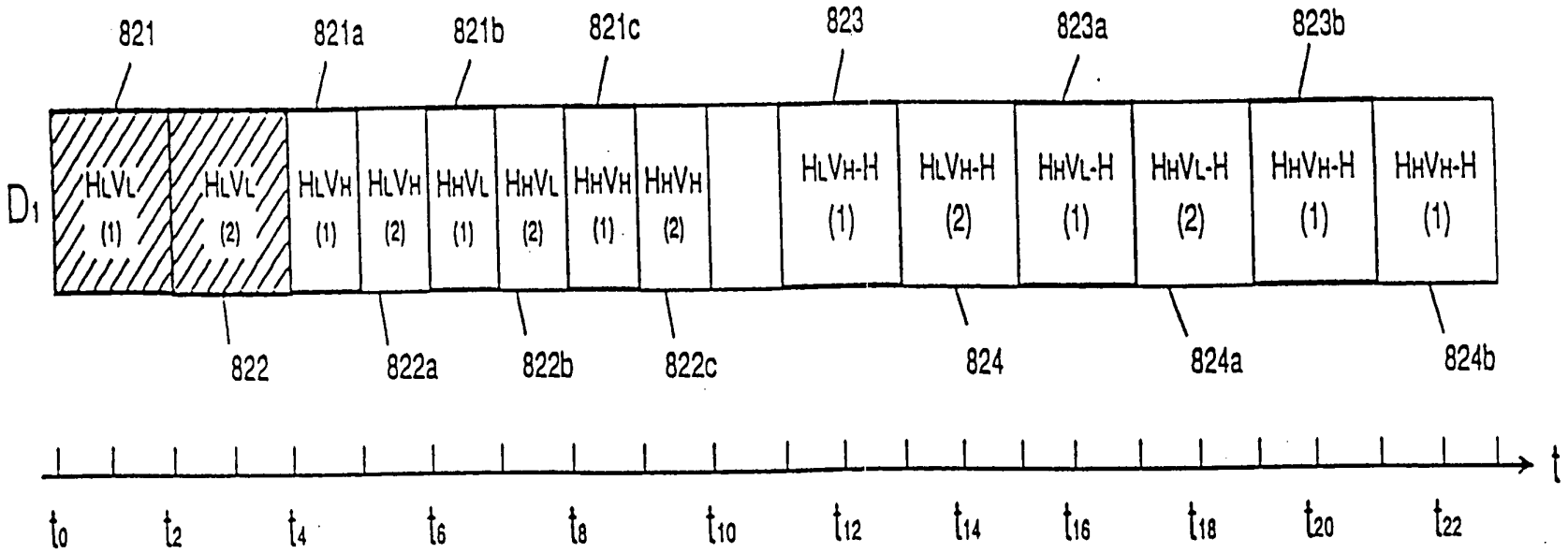

821
821a
821b
821c
823
823a
823b
D1
HLVL (1)
HLVL (2)
HLVH (1)
HLVH (2)
HHVL (1)
HHVL (2)
HHVH (1)
HHVH (2)
HLVH-H (1)
HLVH-H (2)
HHVL-H (1)
HHVL-H (2)
HHVH-H (1)
HHVH-H (1)
822
822a
822b
822c
824
824a
824b
t
t0
t2
t4
t6
t8
t10
t12
t14
t16
t18
t20
t22

FIG. 82

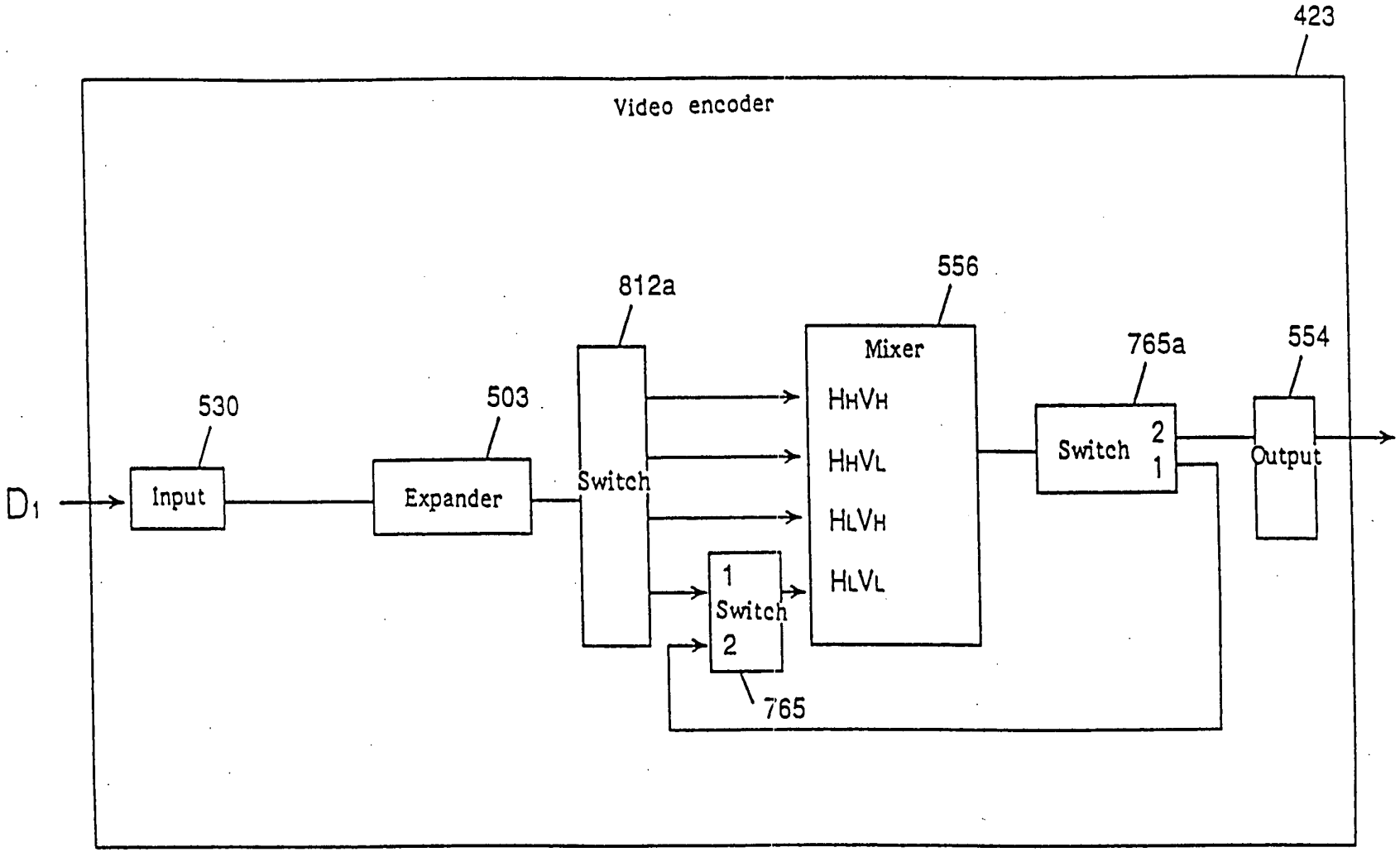

423
Video encoder
812a
556
Mixer
765a
554
530
503
D1
Input
Expander
Switch
HHVH
HHVL
HLVH
HLVL
Switch 2 1
Output
1
Switch
2
765

FIG. 83

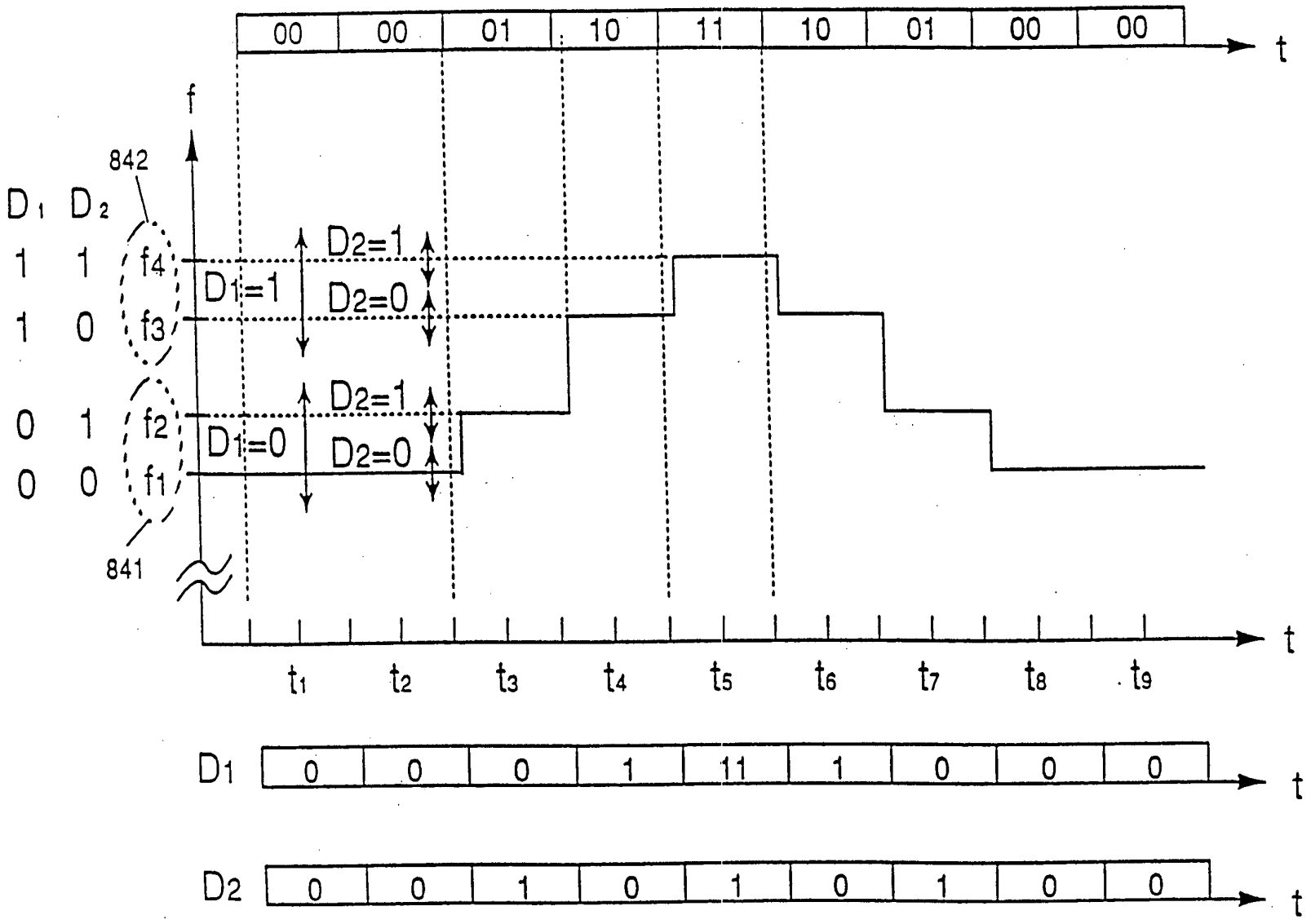

00 00 01 10 11 10 01 00 00
t
f
842
D1 D2
1 1
1 0
0 1
0 0
f4
f3
f2
f1
841
D1=1
D1=0
D2=1
D2=0
D2=1
D2=0
t
t1 t2 t3 t4 t5 t6 t7 t8 t9
D1
0 0 0 1 11 1 0 0 0
t
D2
0 0 1 0 1 0 1 0 0
t

FIG. 84

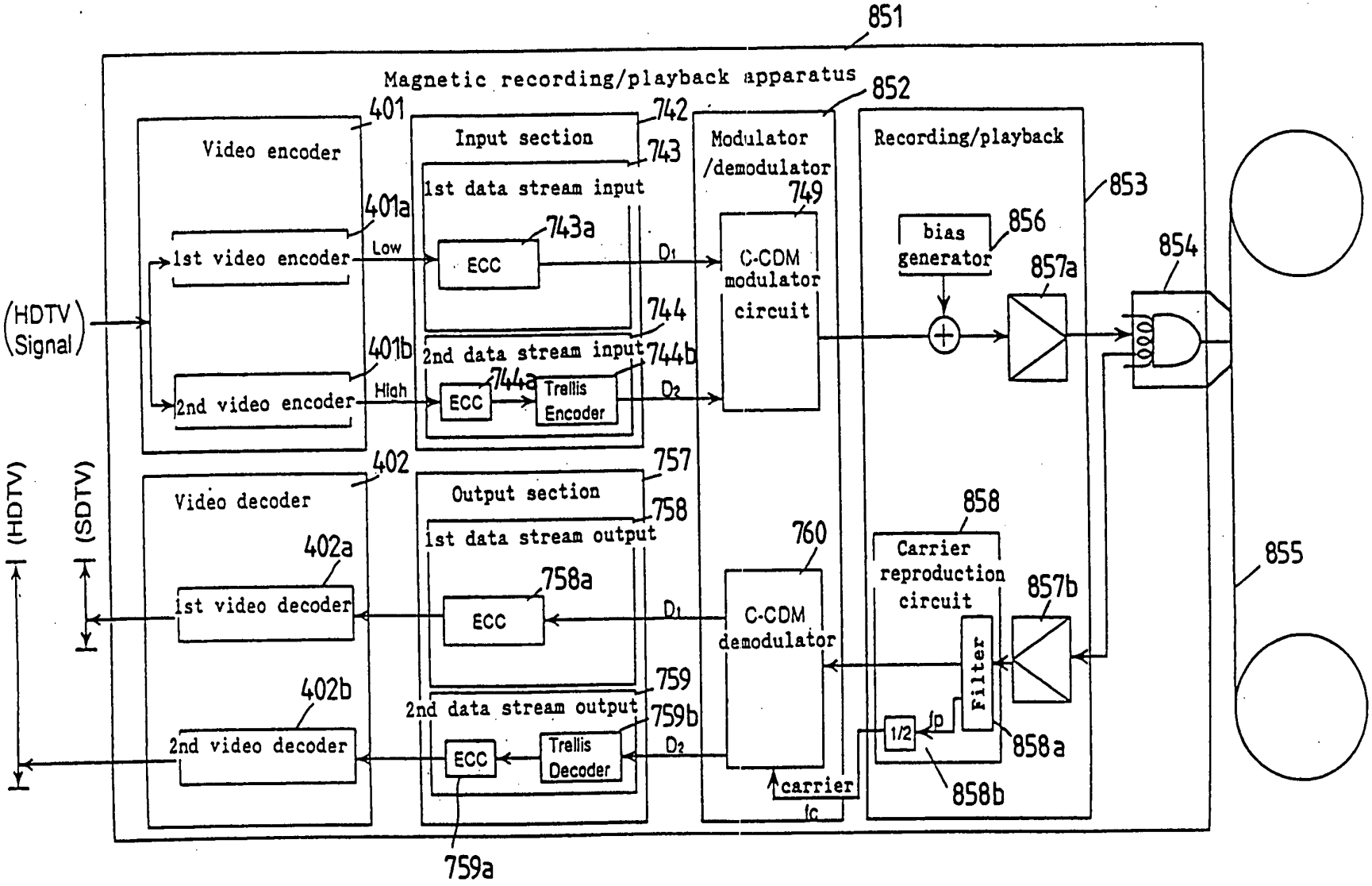

851
Magnetic recording/playback apparatus
852
401
Video encoder
742
Input section
743
Modulator /demodulator
Recording/playback
853
1st data stream input
749
401a
743a
bias generator
856
854
857a
1st video encoder
Low
ECC
D1
C-CDM modulator circuit
744
2nd data stream input
744b
401b
744a
Trellis Encoder
(HDTV Signal)
2nd video encoder
High
ECC
D2
402
757
Video decoder
Output section
758
1st data stream output
858
760
Carrier reproduction circuit
855
402a
758a
857b
1st video decoder
ECC
D1
C-CDM demodulator
Filter
759
402b
2nd data stream output
759b
1/2
fp
858a
2nd video decoder
ECC
Trellis Decoder
D2
carrier
fc
858b
759a
(HDTV)
(SDTV)

FIG. 85

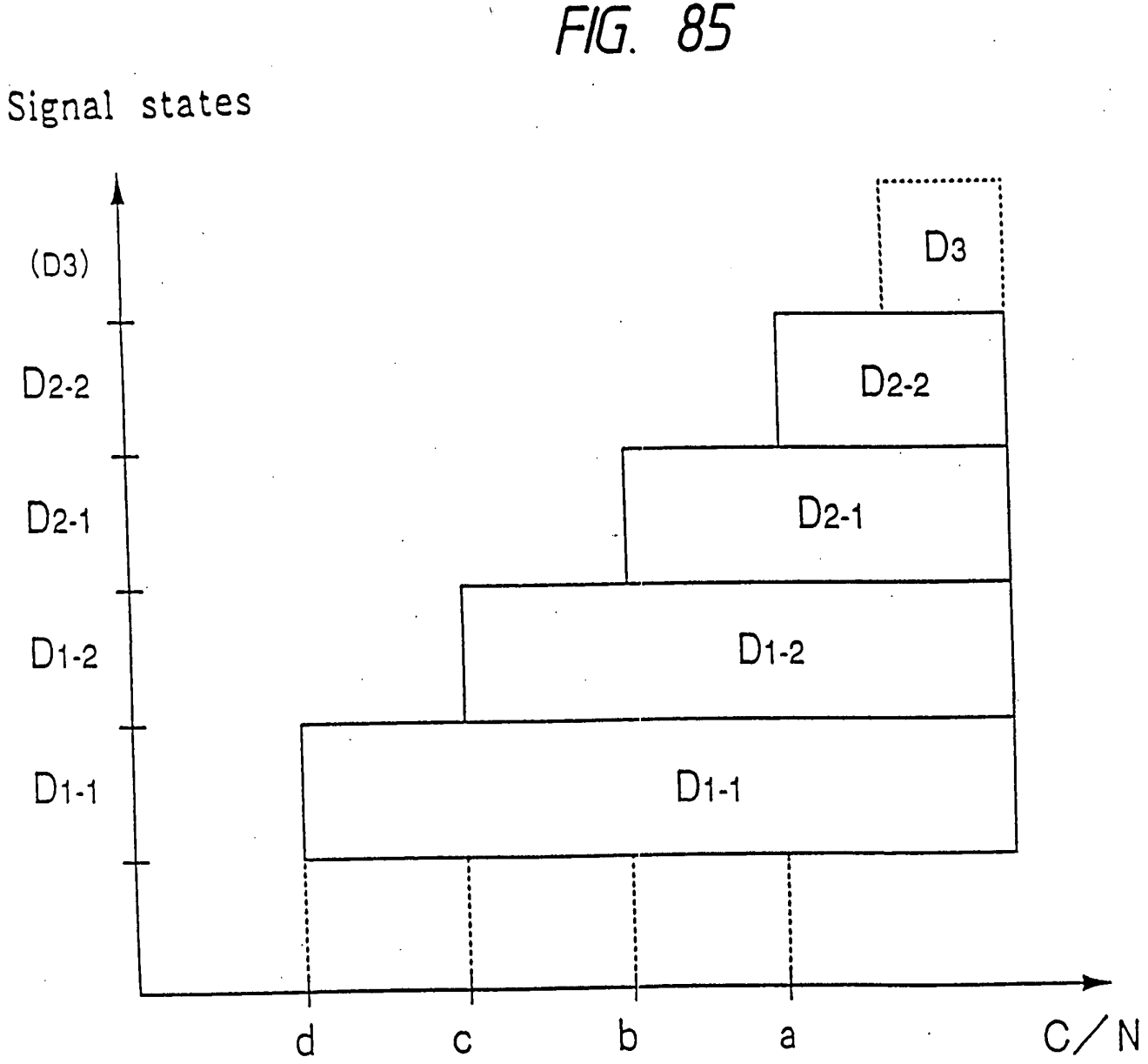


FIG. 86

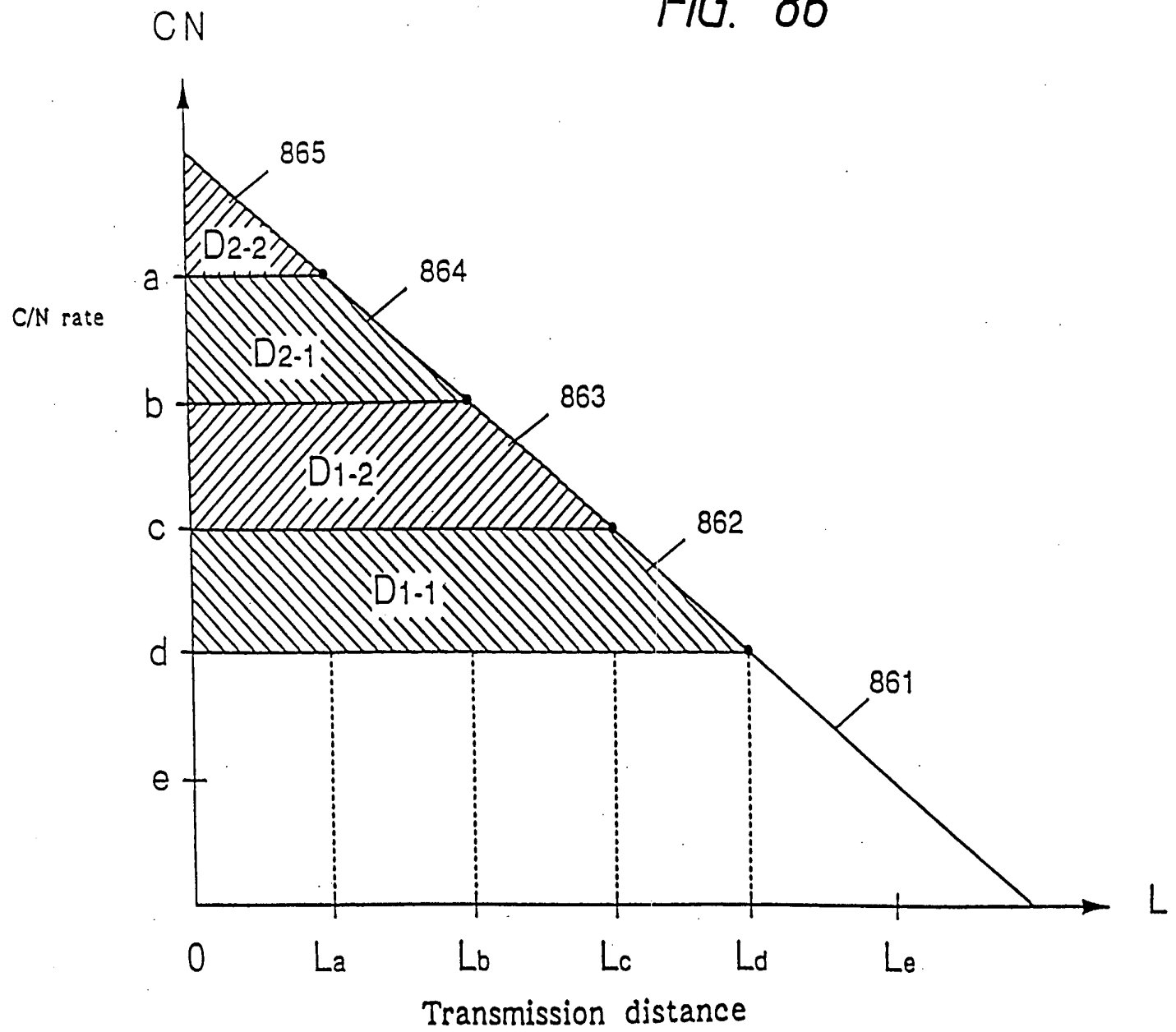

CN
865
D2-2
a
C/N rate
864
D2-1
b
863
D1-2
c
862
D1-1
d
861
e
L
0
La
Lb
Lc
Ld
Le
Transmission distance

FIG. 87

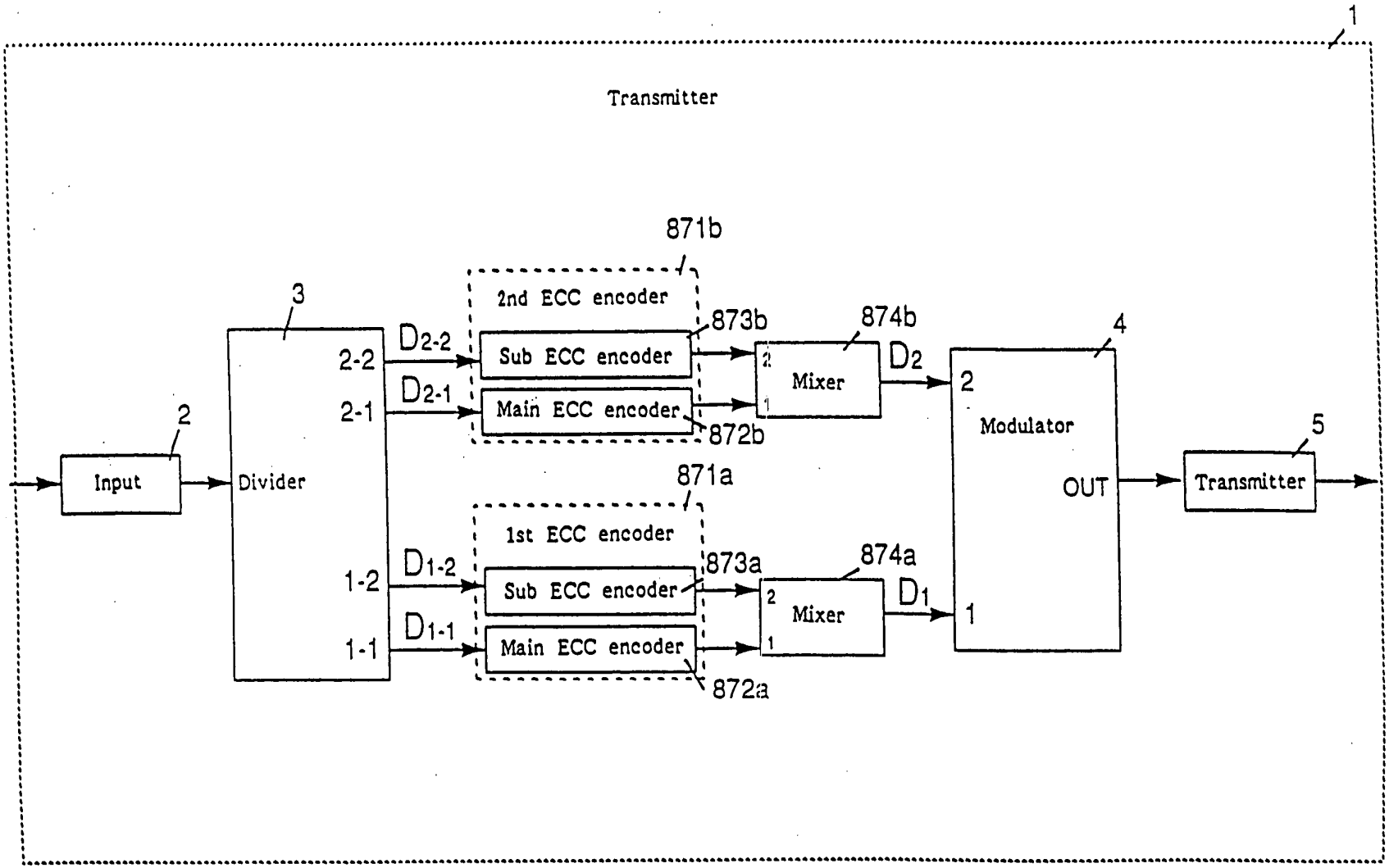

1
Transmitter
871b
2nd ECC encoder
3
D2-2
2-2
Sub ECC encoder
873b
874b
Mixer
D2
4
D2-1
2-1
Main ECC encoder
872b
2
Modulator
2
Input
Divider
OUT
5
Transmitter
871a
1st ECC encoder
D1-2
1-2
Sub ECC encoder
873a
874a
Mixer
D1
1
D1-1
1-1
Main ECC encoder
872a

FIG. 88

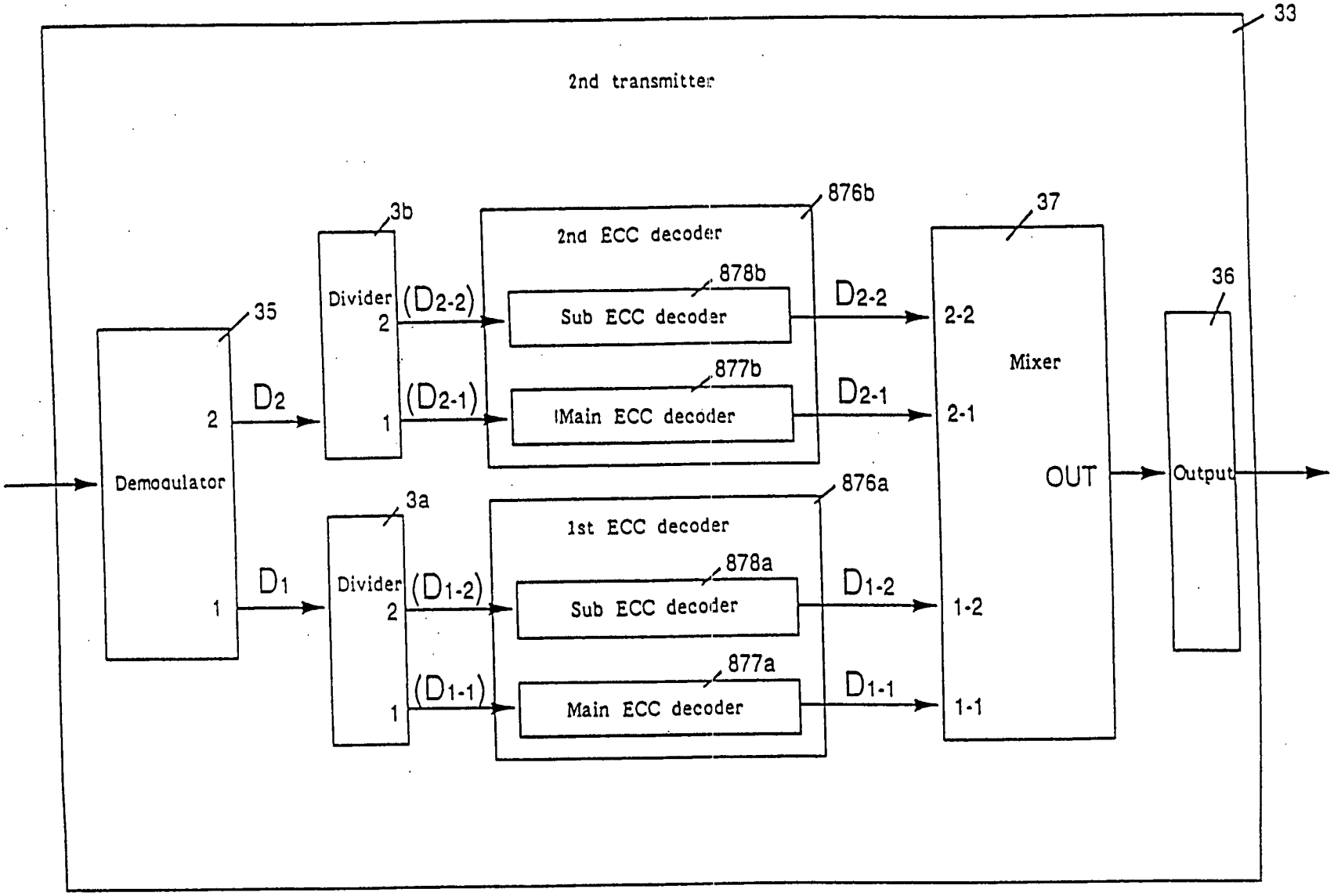

33
2nd transmitter
35
Demodulator
2
1
D2
D1
3b
Divider
2
1
(D2-2)
(D2-1)
3a
Divider
2
1
(D1-2)
(D1-1)
876b
2nd ECC decoder
878b
Sub ECC decoder
877b
Main ECC decoder
876a
1st ECC decoder
878a
Sub ECC decoder
877a
Main ECC decoder
D2-2
D2-1
D1-2
D1-1
37
2-2
2-1
Mixer
OUT
1-2
1-1
36
Output

FIG. 89

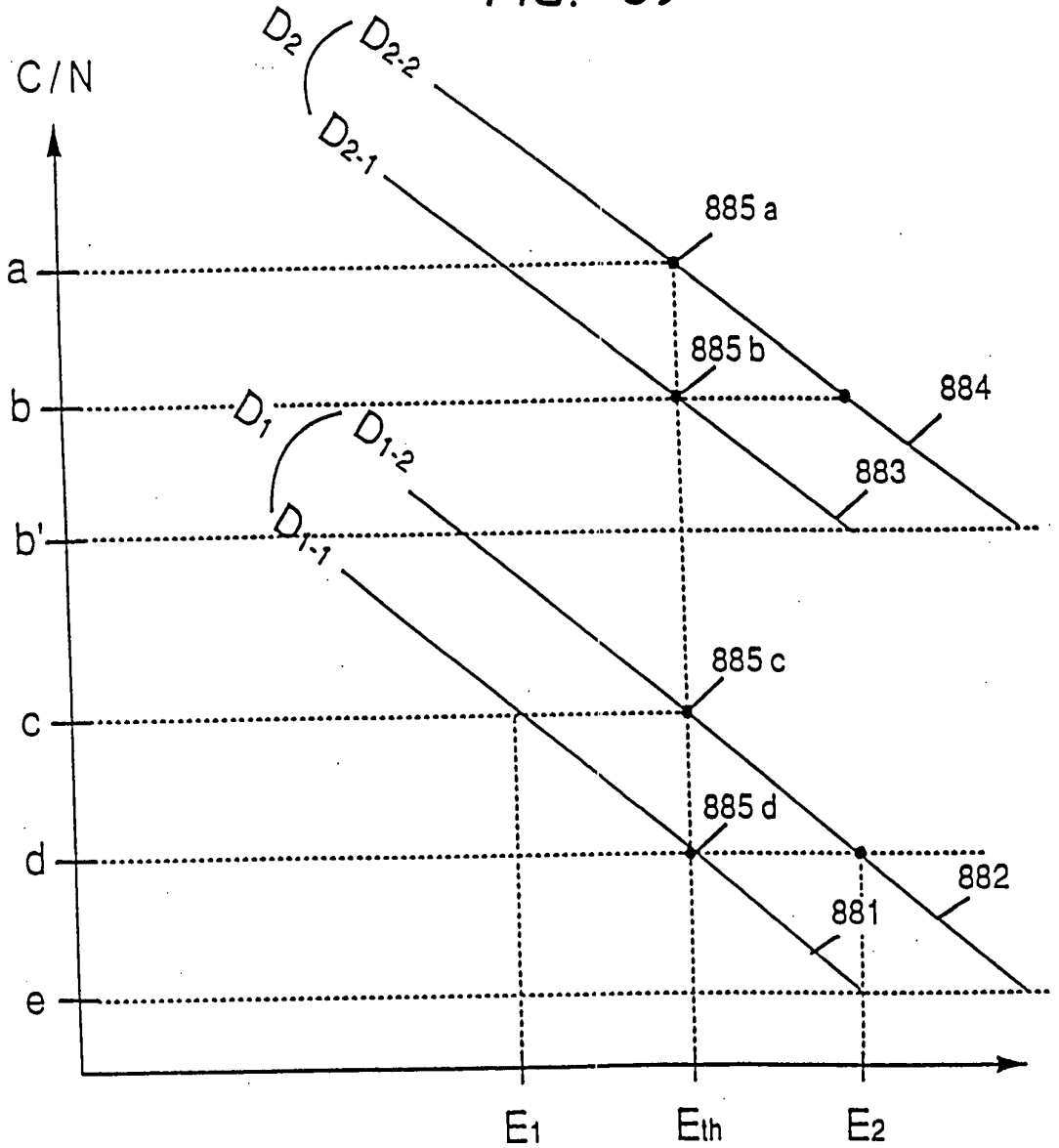

C/N
D2
D2-2
D2-1
885 a
a
885 b
884
b
D1
D1-2
883
b'
D1-1
885 c
c
885 d
d
882
881
e
E1
Eth
E2
Error rate after error correction

FIG. 90

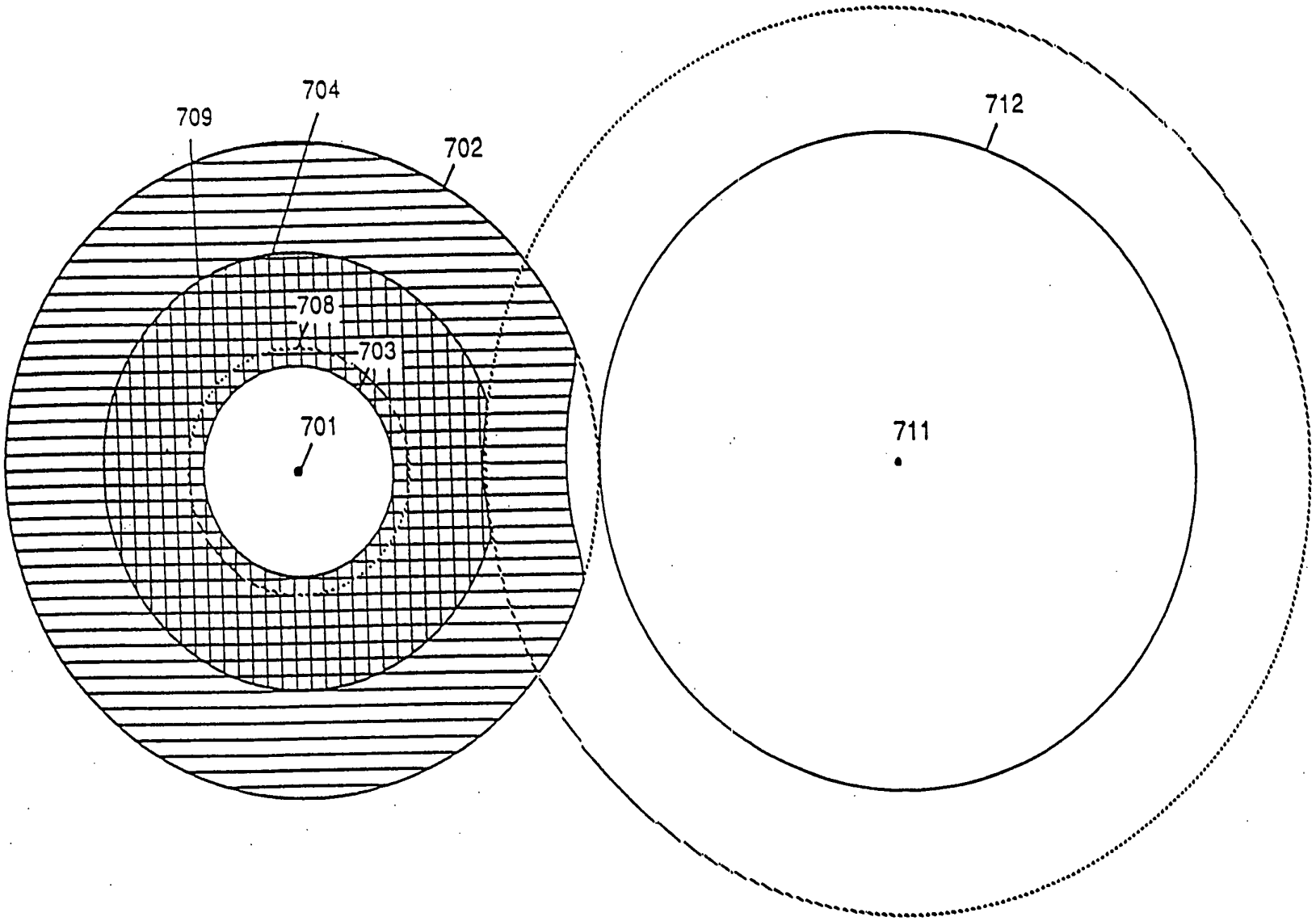


FIG. 91

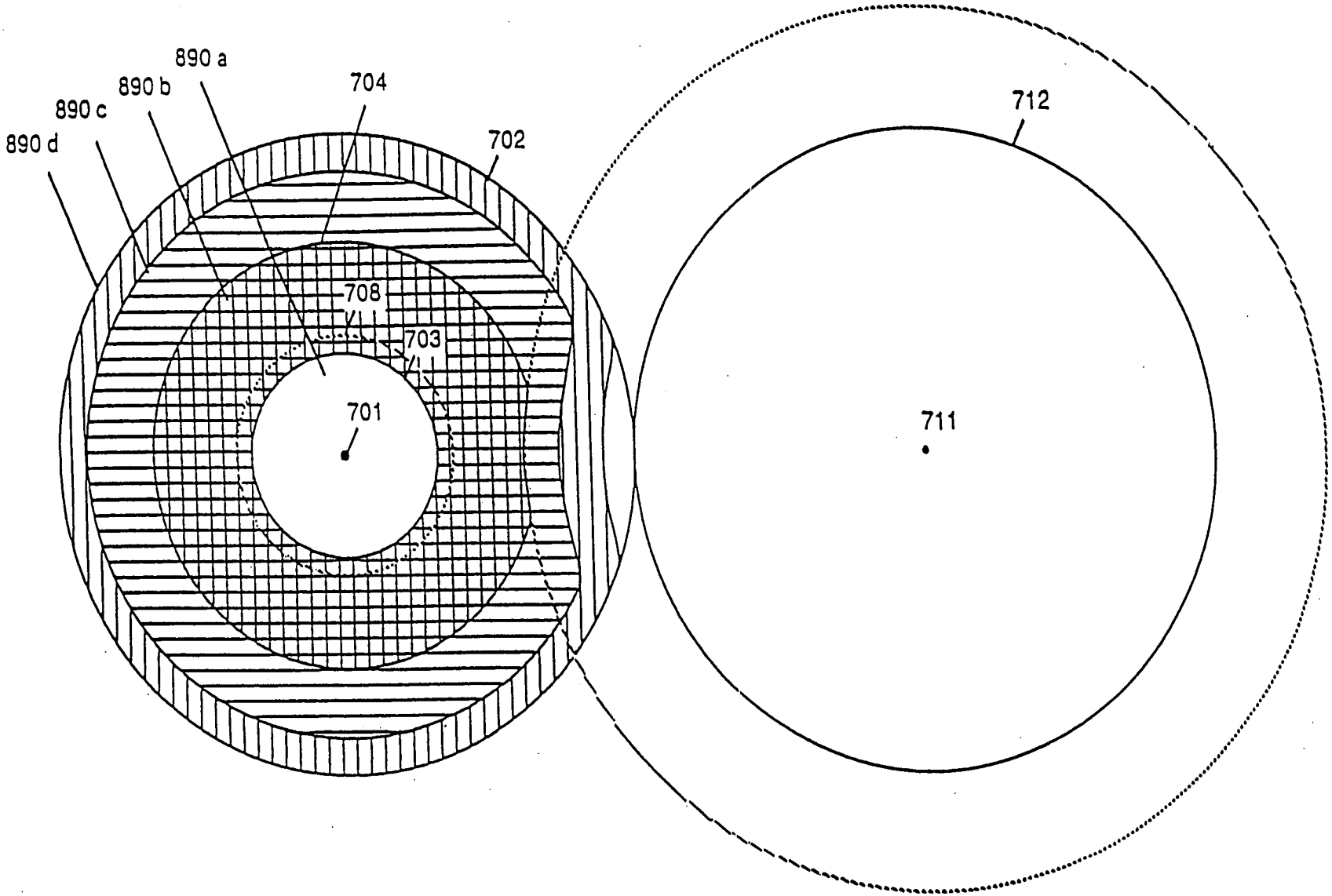


FIG. 92

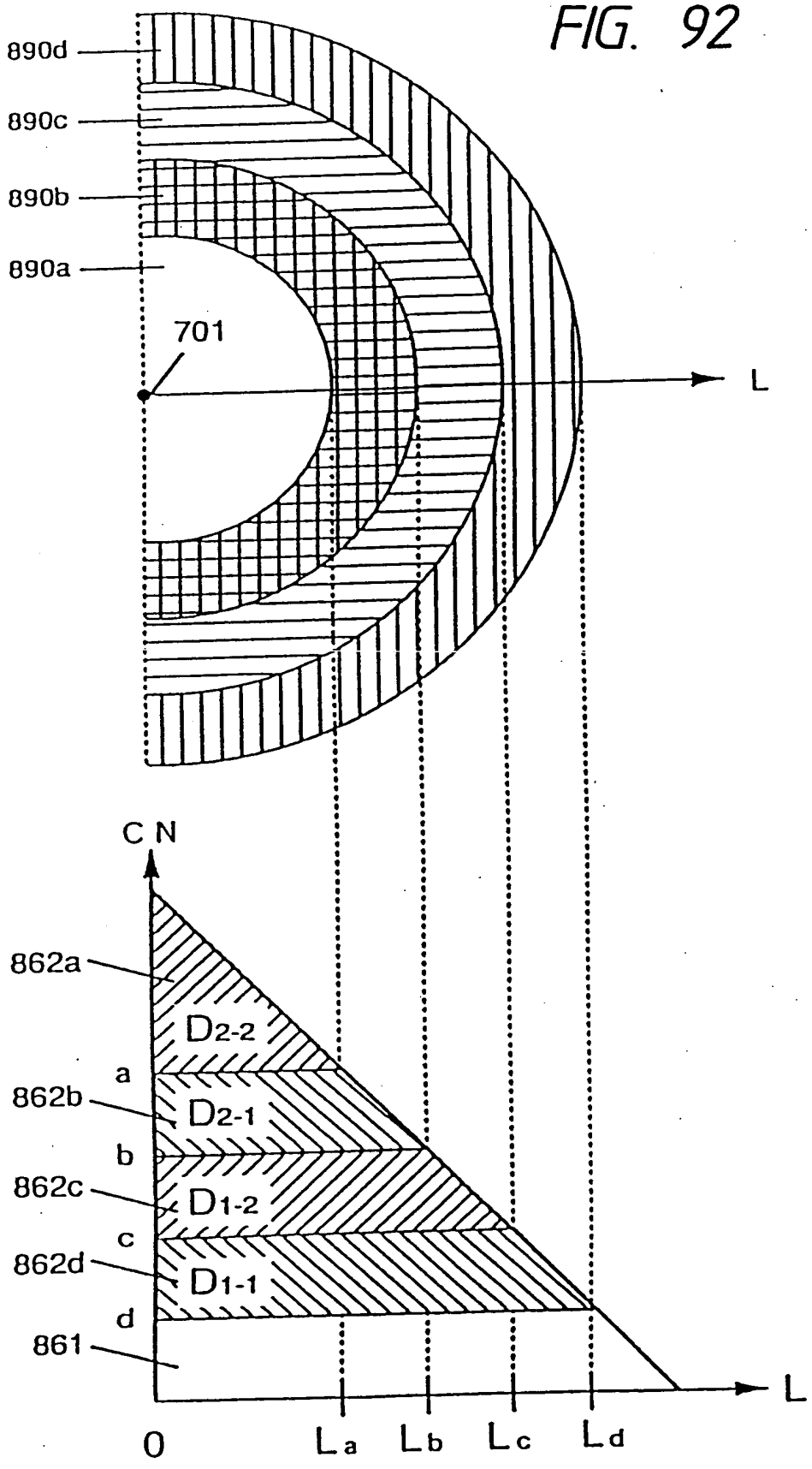

890d
890c
890b
890a
701
L
C N
862a
D2-2
a
862b
D2-1
b
862c
D1-2
c
862d
D1-1
d
861
L
0
La
Lb
Lc
Ld

FIG. 93

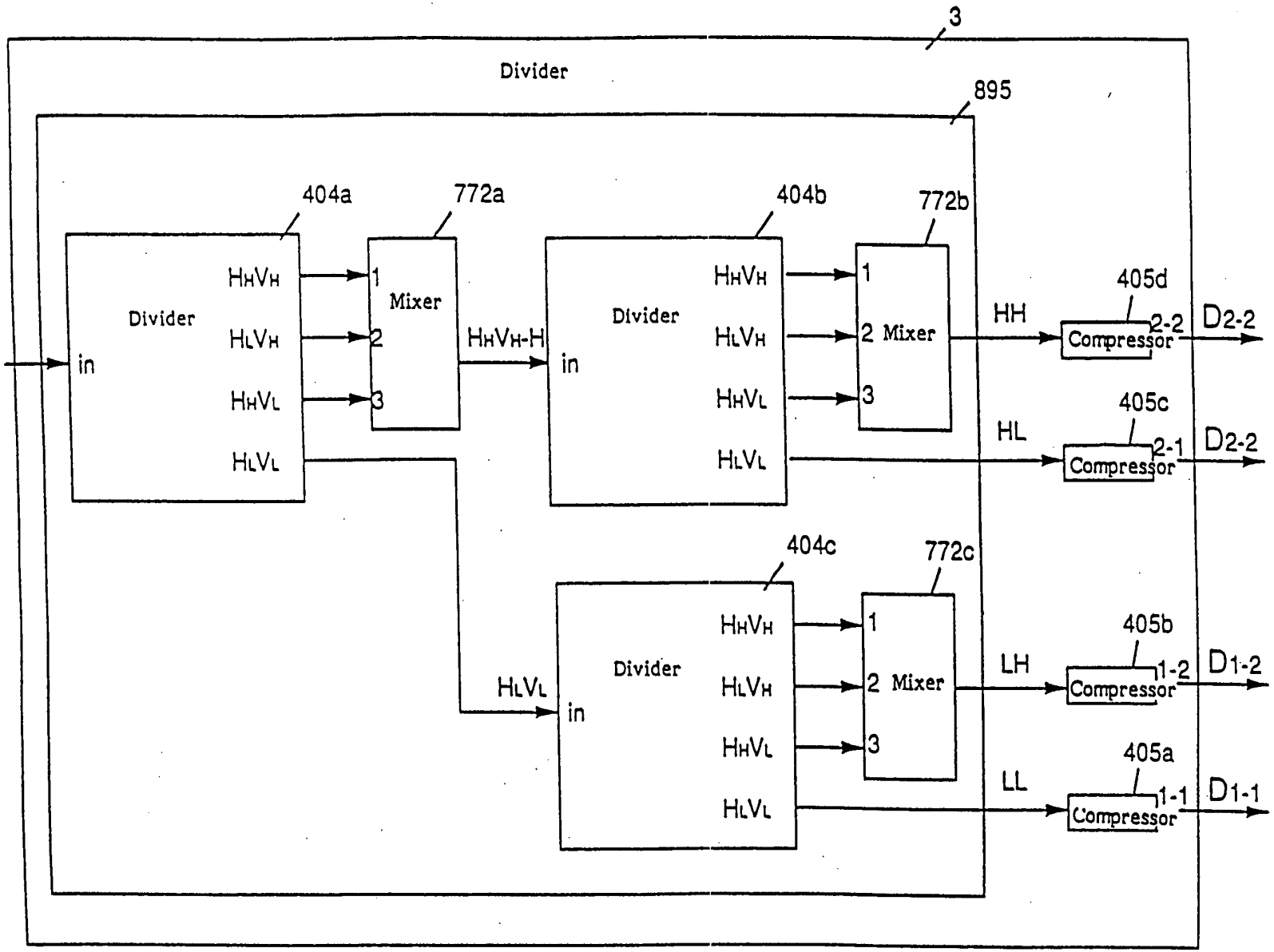

3
Divider
895
404a
772a
404b
772b
Divider
in
HHVH
HLVH
HHVL
HLVL
1
2
3
Mixer
HHVH-H
Divider
in
HHVH
HLVH
HHVL
HLVL
1
2 Mixer
3
HH
405d
Compressor
2-2
D2-2
HL
405c
Compressor
2-1
D2-2
404c
772c
HLVL
Divider
in
HHVH
HLVH
HHVL
HLVL
1
2 Mixer
3
LH
405b
Compressor
1-2
D1-2
LL
405a
Compressor
1-1
D1-1

FIG. 94

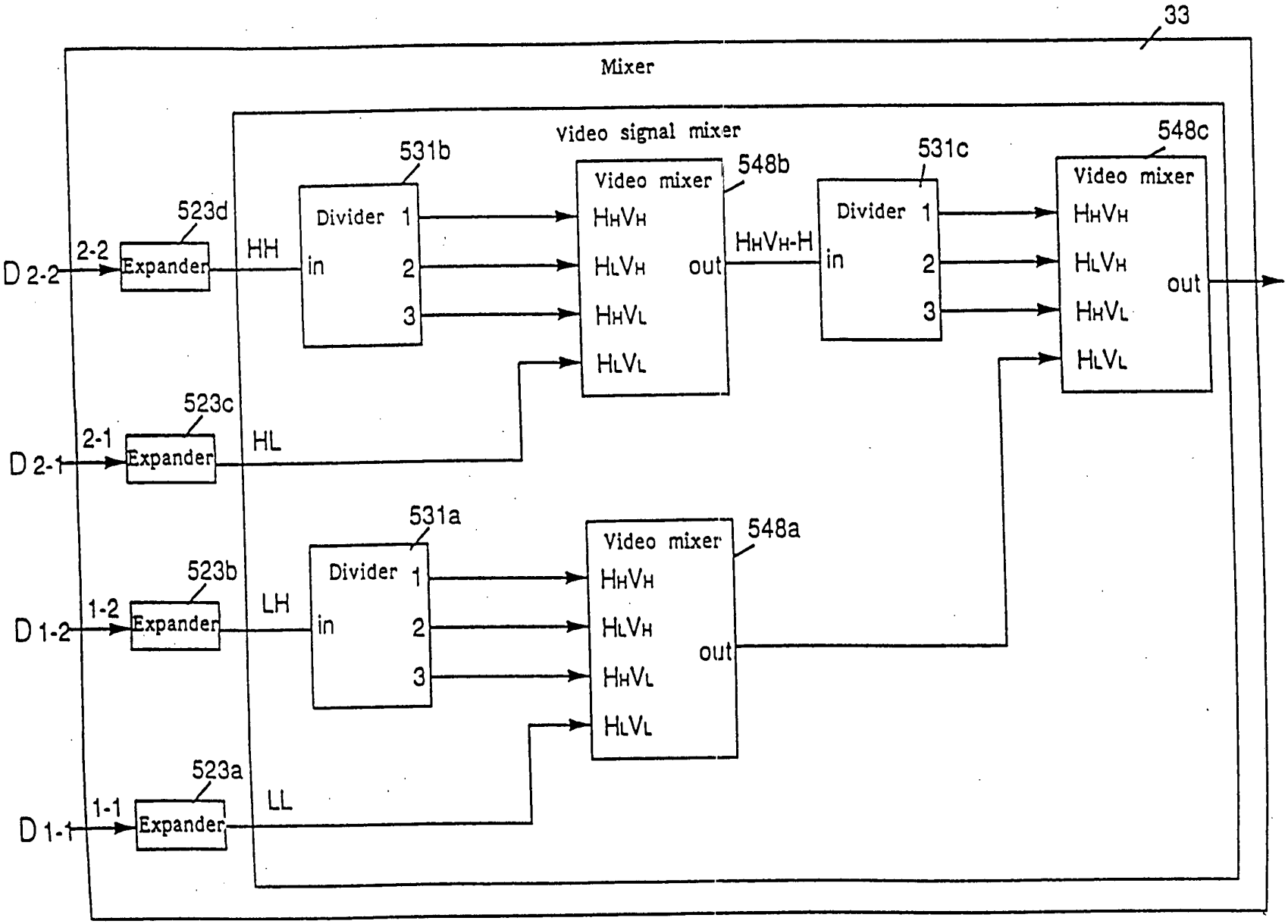

33
Mixer
Video signal mixer
531b
Divider
1
2
3
in
548b
Video mixer
HHVH
HLVH
HHVL
HLVL
out
HHVH-H
531c
Divider
1
2
3
in
548c
Video mixer
HHVH
HLVH
HHVL
HLVL
out
523d
Expander
2-2
D 2-2
HH
523c
Expander
2-1
D 2-1
HL
531a
Divider
1
2
3
in
548a
Video mixer
HHVH
HLVH
HHVL
HLVL
out
523b
Expander
1-2
D 1-2
LH
523a
Expander
1-1
D 1-1
LL

FIG. 95

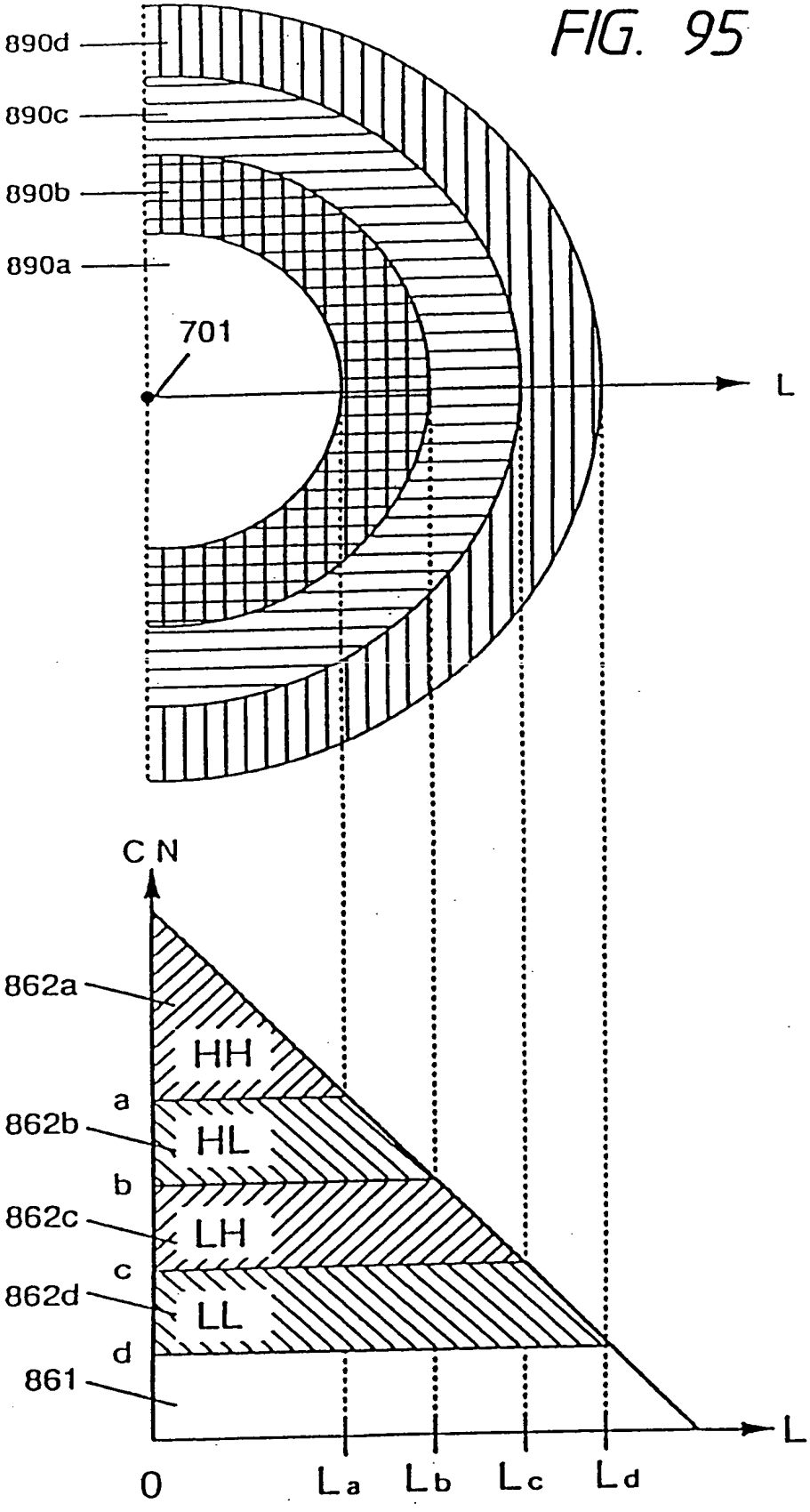

890d
890c
890b
890a
701
L
C N
862a
HH
a
862b
HL
b
862c
LH
c
862d
LL
d
861
L
0
La
Lb
Lc
Ld

FIG. 96

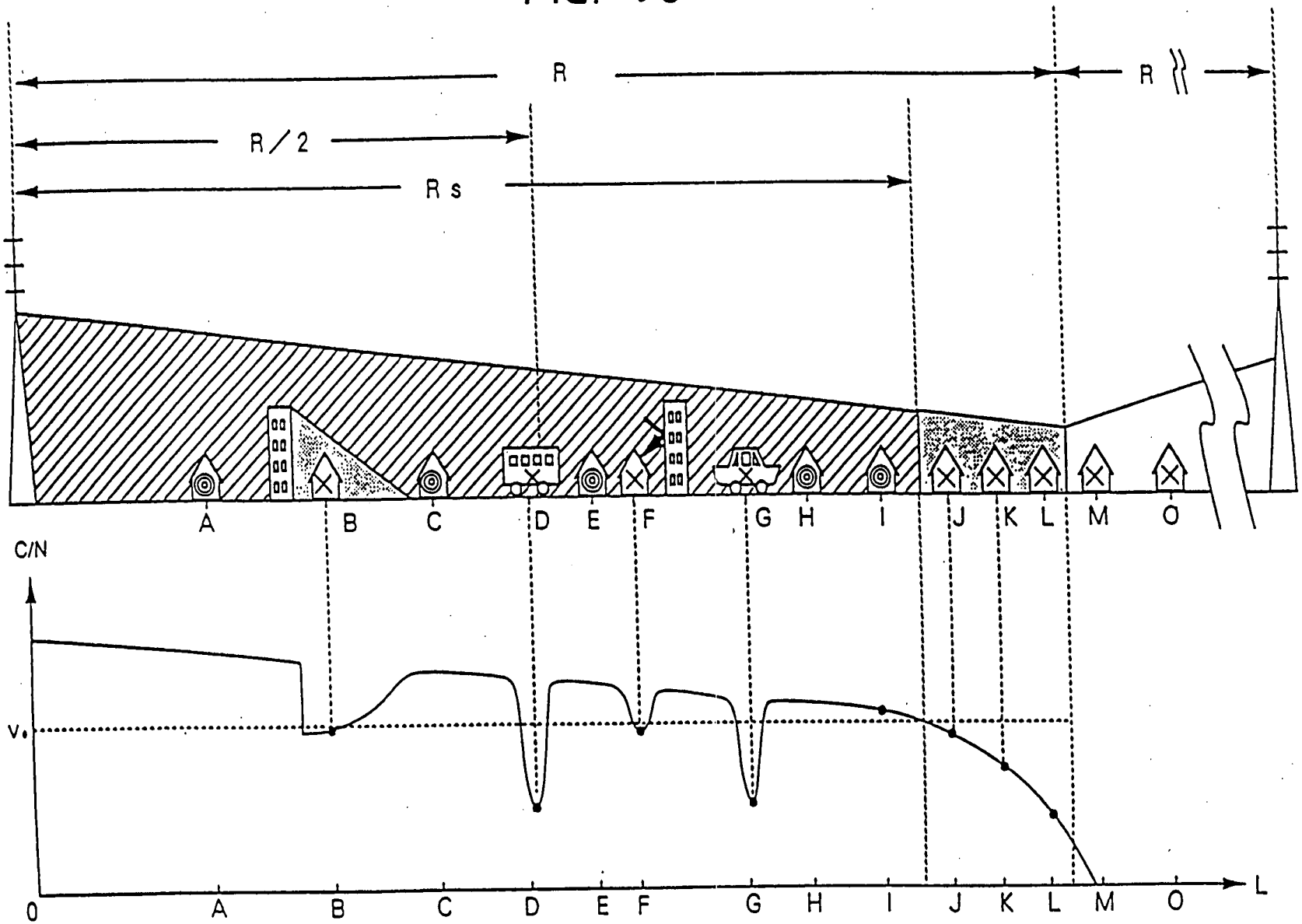


FIG. 97

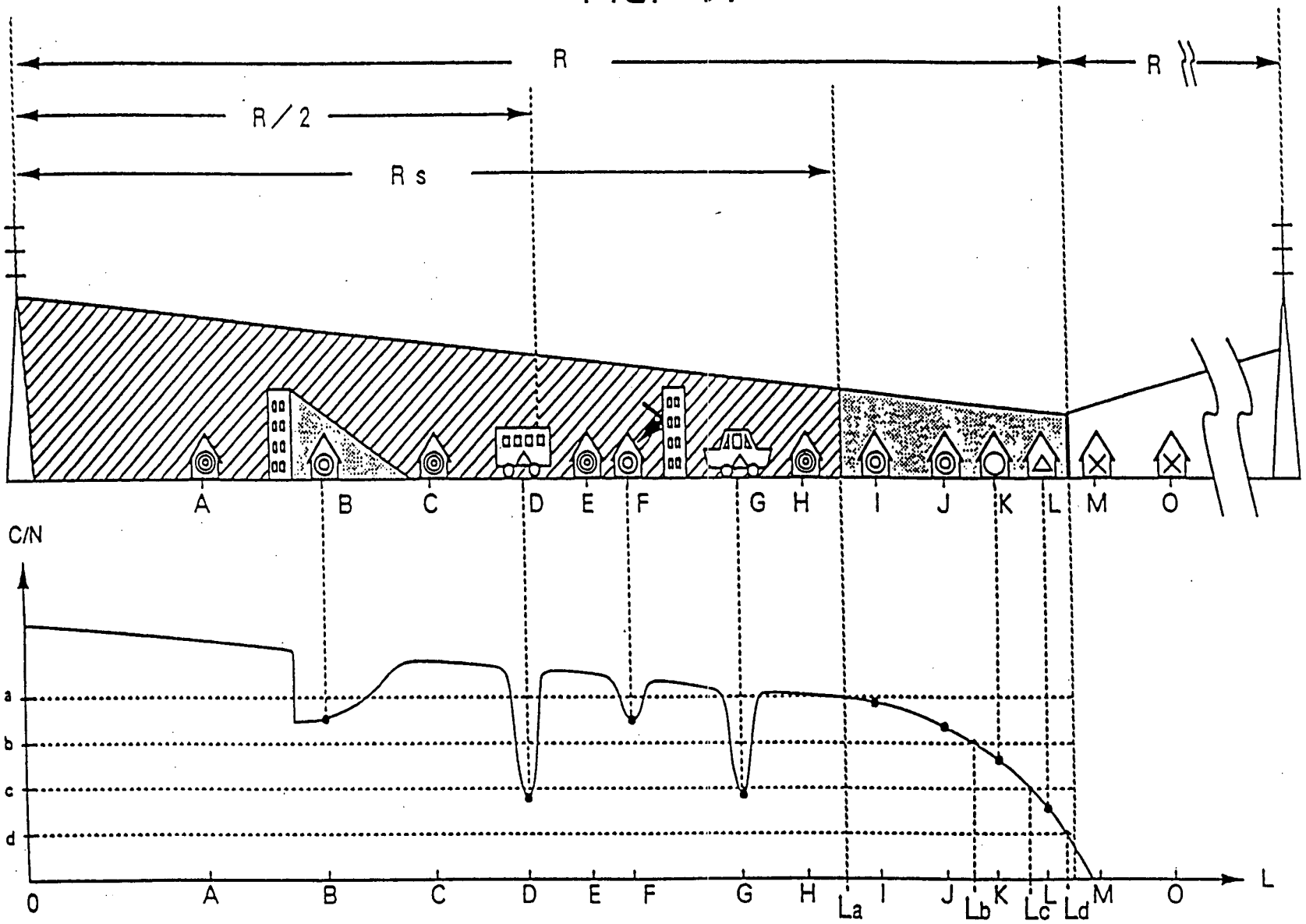

R
R
R / 2
R s
A
B
C
D
E
F
G
H
I
J
K
L
M
O
C/N
a
b
c
d
0
A
B
C
D
E
F
G
H
La
I
J
Lb
K
Lc
L
Ld
M
O
L

FIG. 98

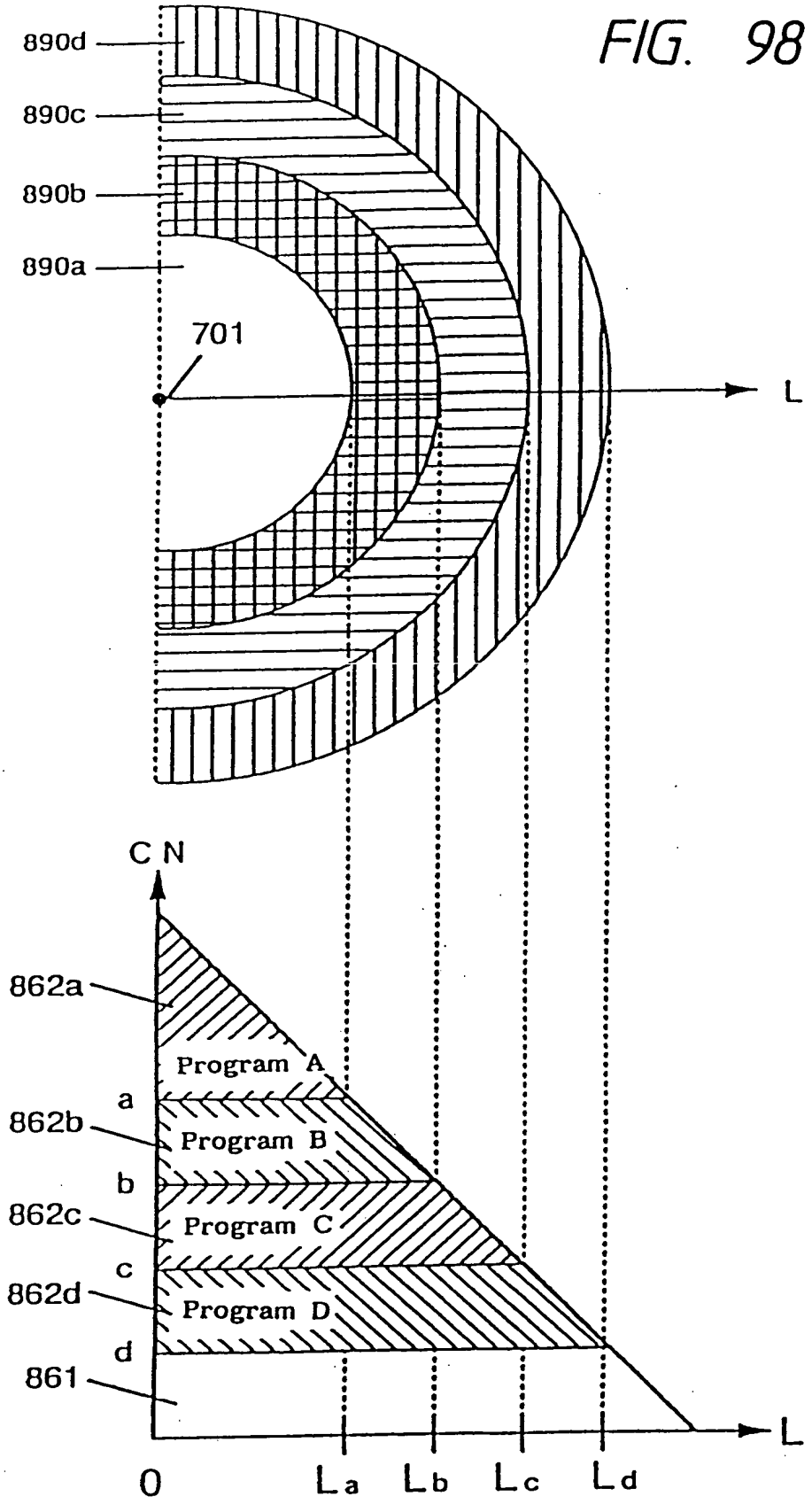

890d
890c
890b
890a
701
L
C N
862a
Program A
a
862b
Program B
b
862c
Program C
c
862d
Program D
d
861
L
0
La
Lb
Lc
Ld

FIG. 99

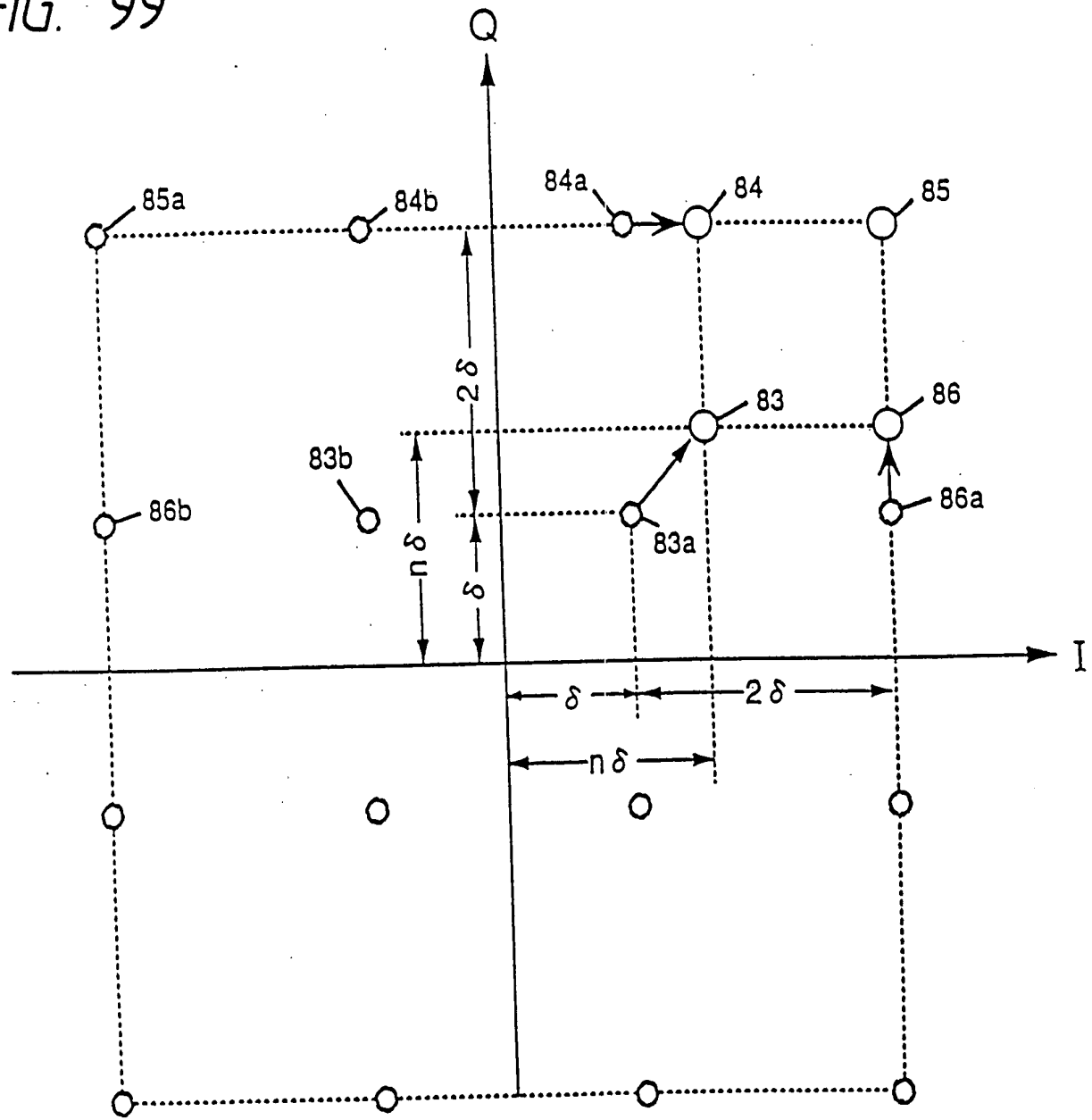


FIG. 100

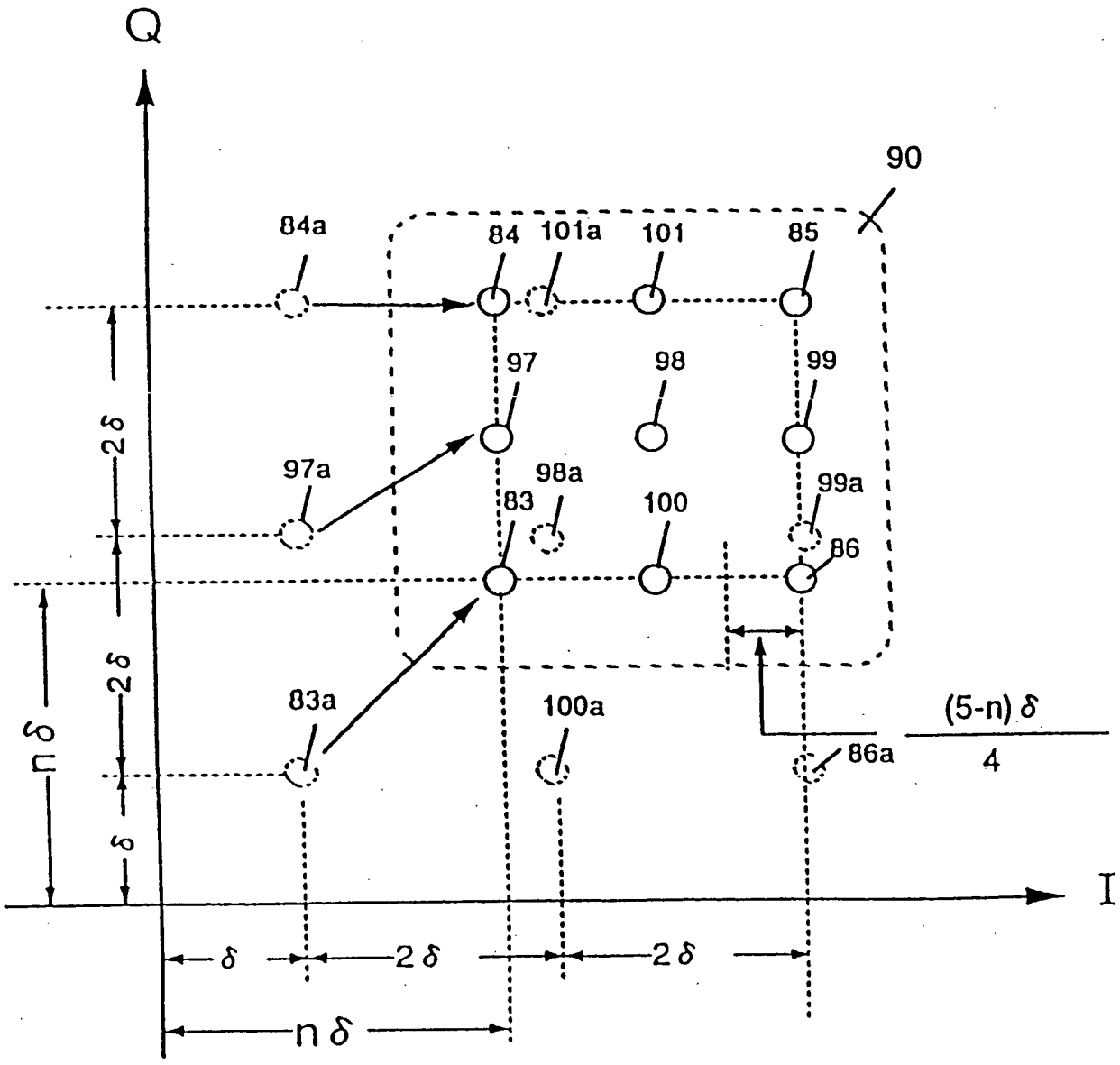

Q
I
90
84a
84
101a
101
85
97
98
99
97a
98a
99a
83
100
86
83a
100a
86a
2δ
2δ
nδ
δ
δ
2δ
2δ
nδ
(5-n)δ
4

FIG. 101

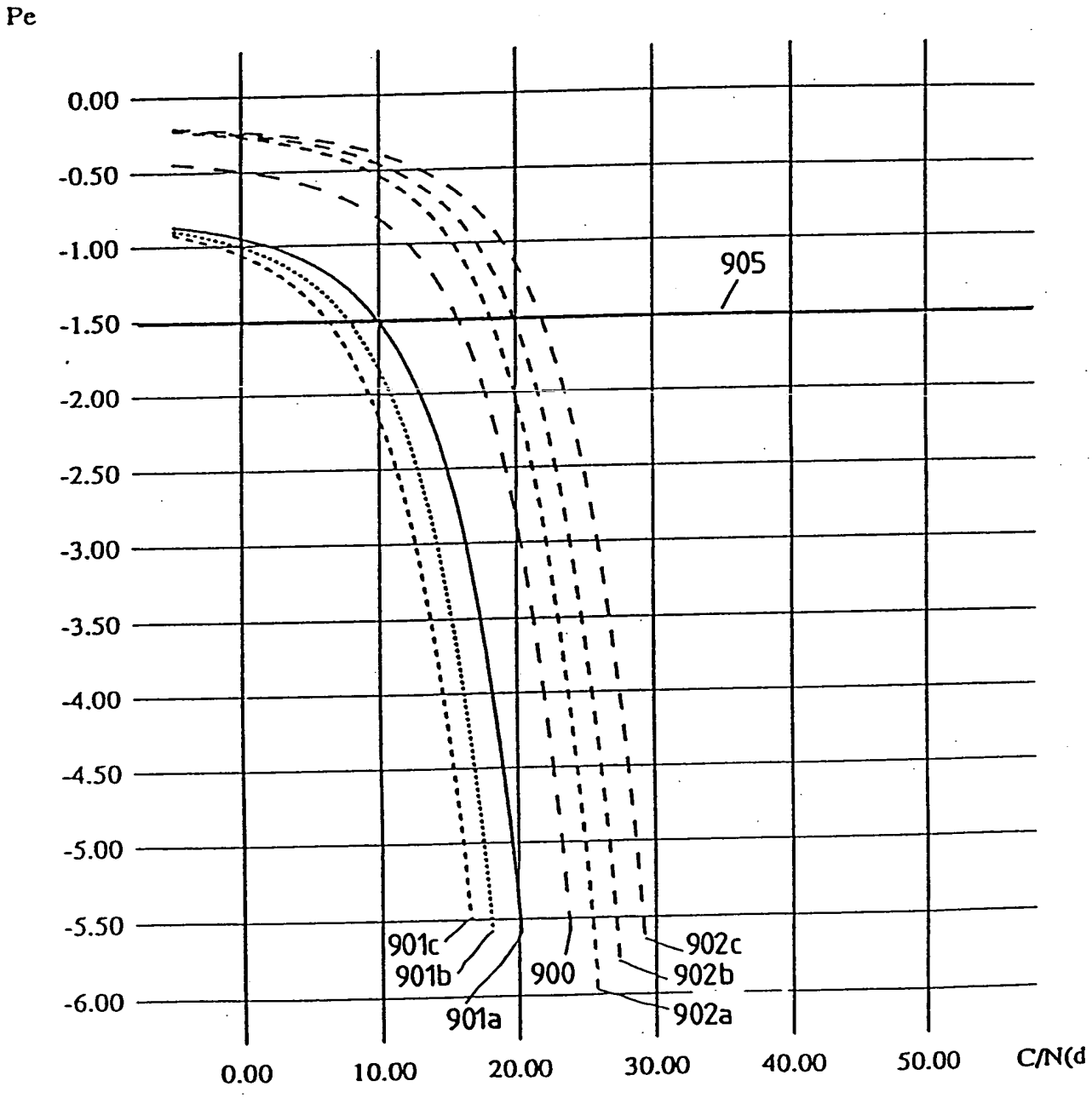

Pe
0.00
-0.50
-1.00
-1.50
-2.00
-2.50
-3.00
-3.50
-4.00
-4.50
-5.00
-5.50
-6.00
905
901c
901b
901a
900
902c
902b
902a
0.00
10.00
20.00
30.00
40.00
50.00
C/N(d

FIG. 102

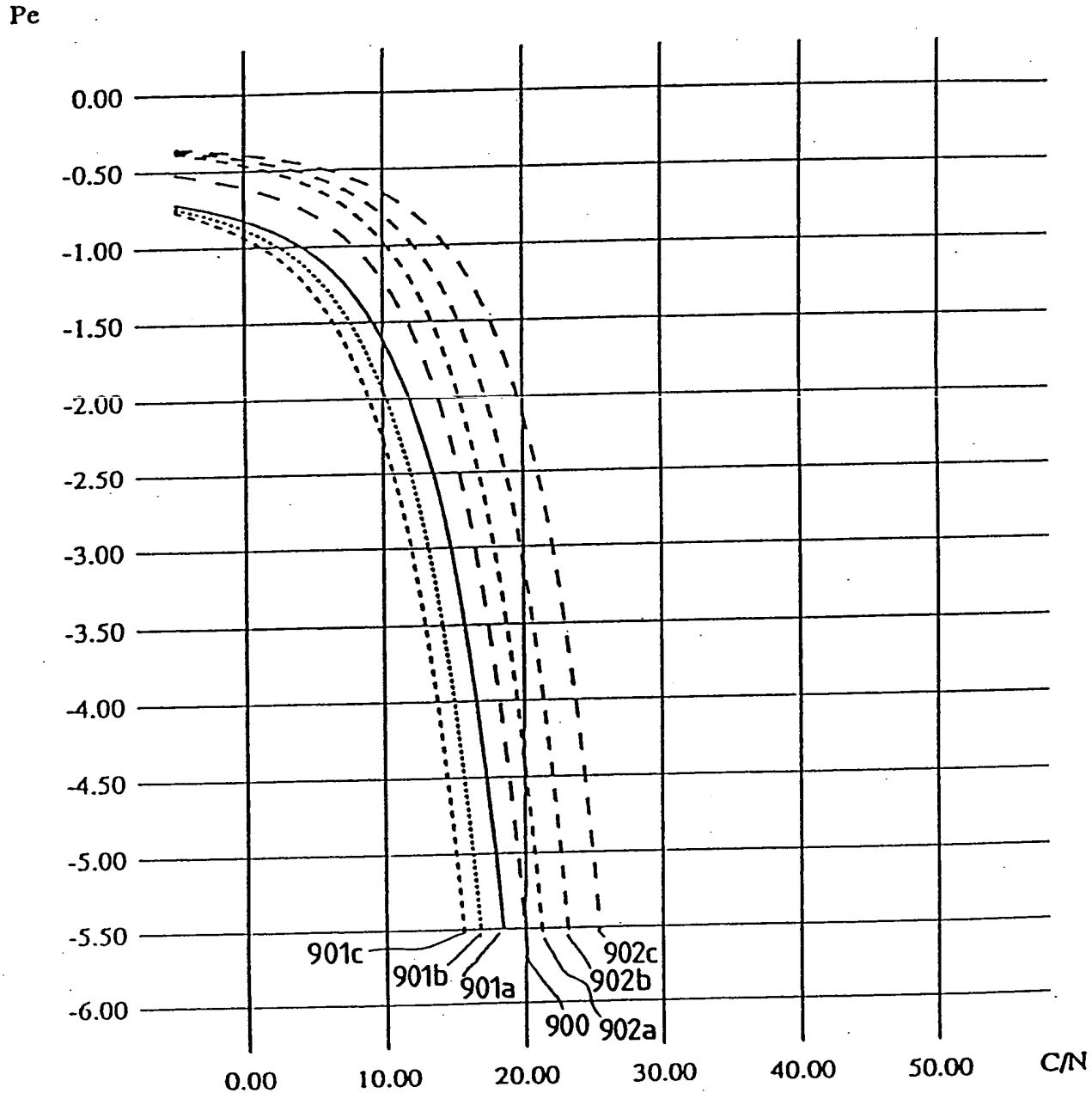

Pe
0.00
-0.50
-1.00
-1.50
-2.00
-2.50
-3.00
-3.50
-4.00
-4.50
-5.00
-5.50
-6.00
0.00
10.00
20.00
30.00
40.00
50.00
C/N
901c
901b
901a
900
902a
902b
902c

FIG. 103

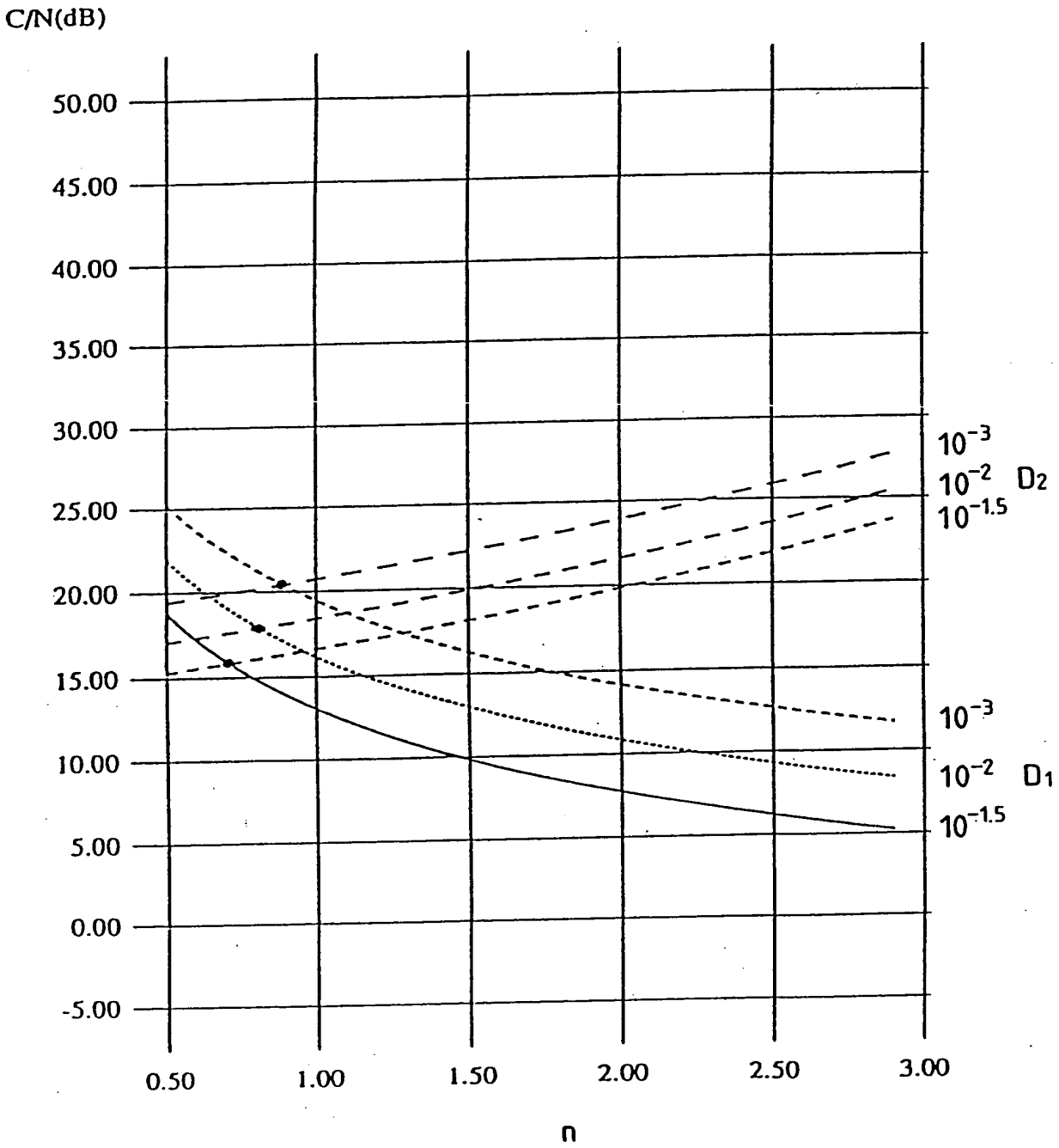

C/N(dB)
50.00
45.00
40.00
35.00
30.00
25.00
20.00
15.00
10.00
5.00
0.00
-5.00
0.50
1.00
1.50
2.00
2.50
3.00
n
10^{-3}
10^{-2}
$10^{-1.5}$
D2
10^{-3}
10^{-2}
$10^{-1.5}$
D1

FIG. 104

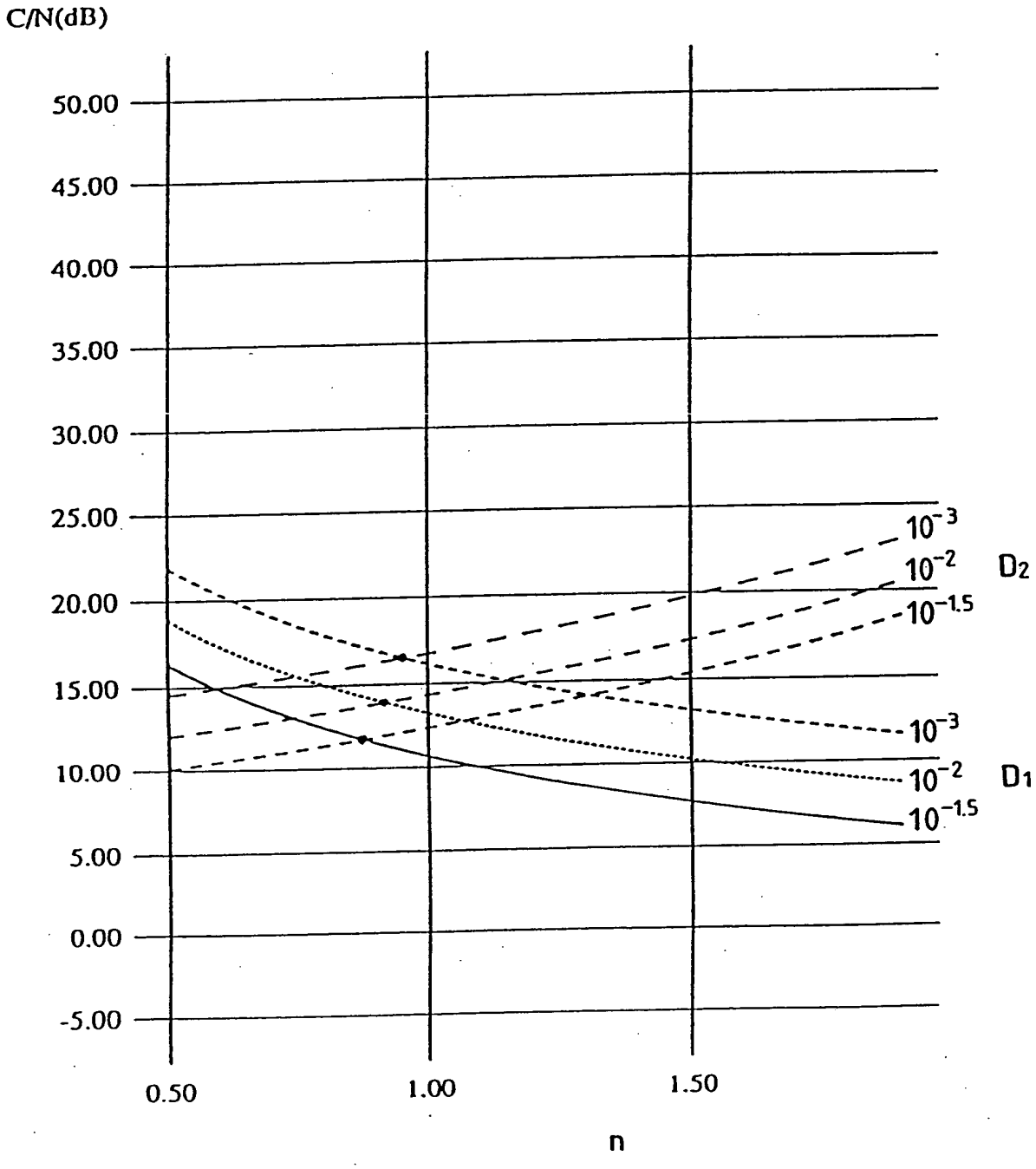

C/N(dB)
50.00
45.00
40.00
35.00
30.00
25.00
20.00
15.00
10.00
5.00
0.00
-5.00
0.50
1.00
1.50
n
10^{-3}
10^{-2}
$10^{-1.5}$
D2
10^{-3}
10^{-2}
$10^{-1.5}$
D1

FIG. 105

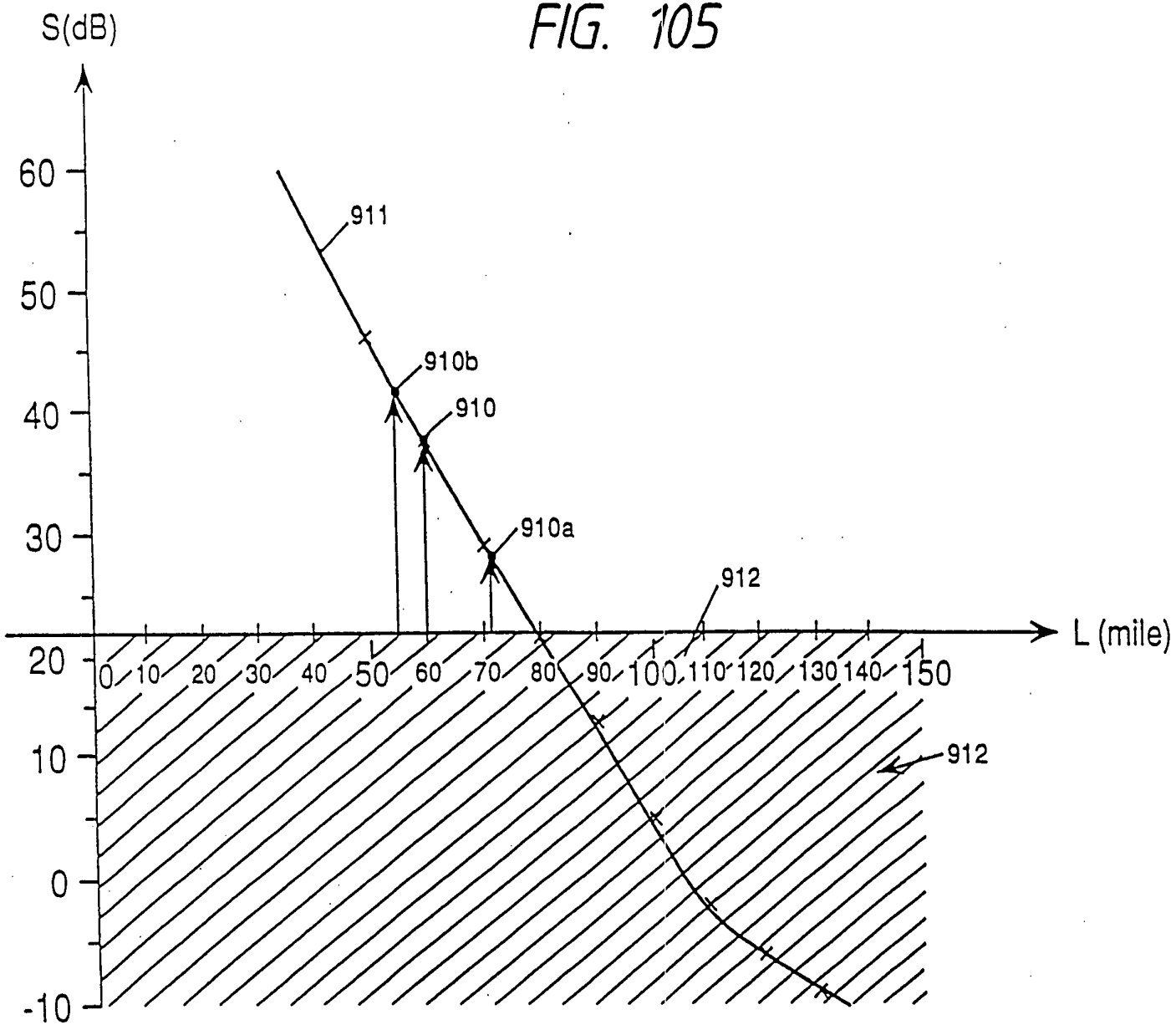

S(dB)
60
50
40
30
20
10
0
-10
911
910b
910
910a
912
912
L (mile)
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150

FIG. 106

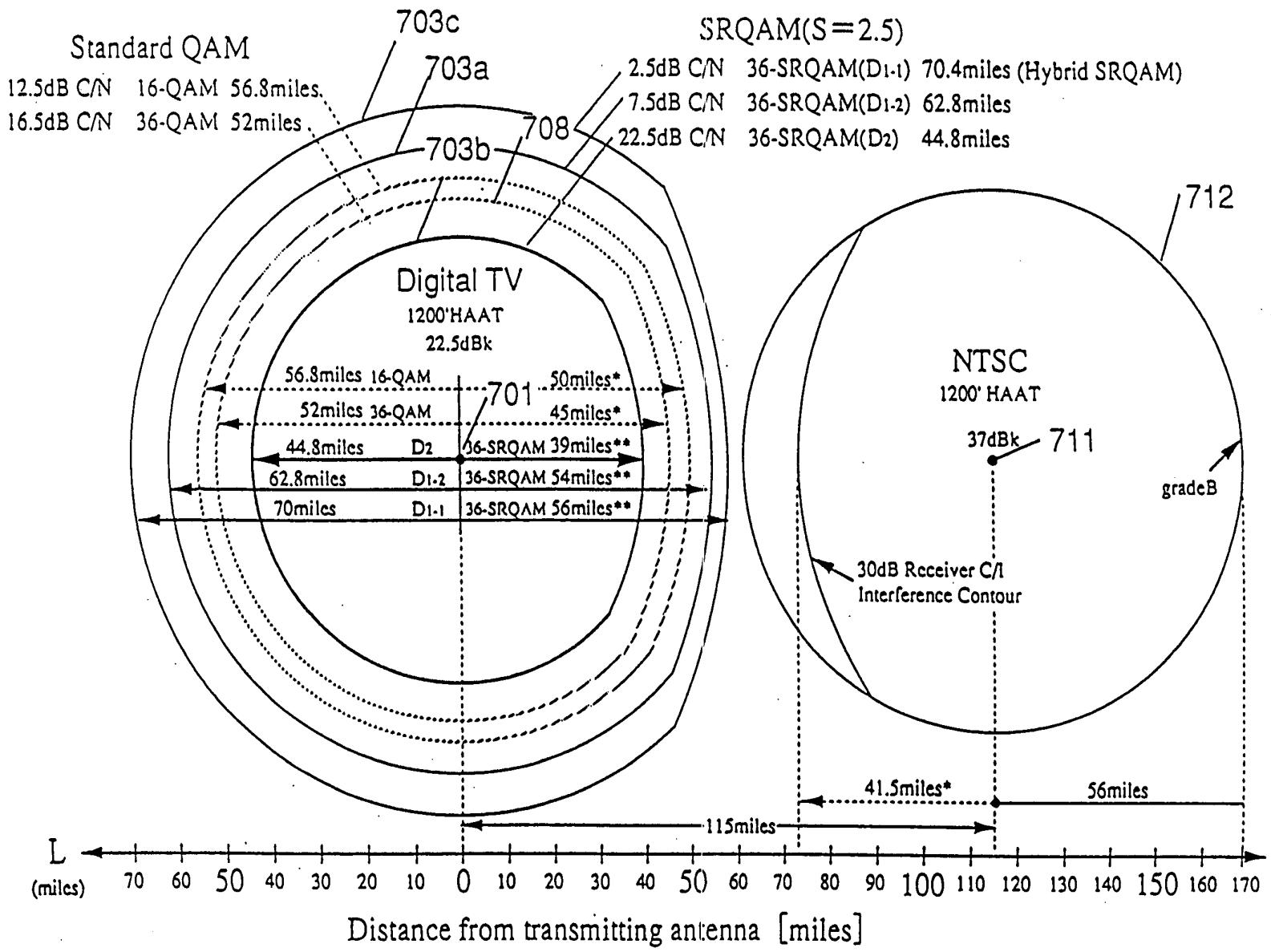
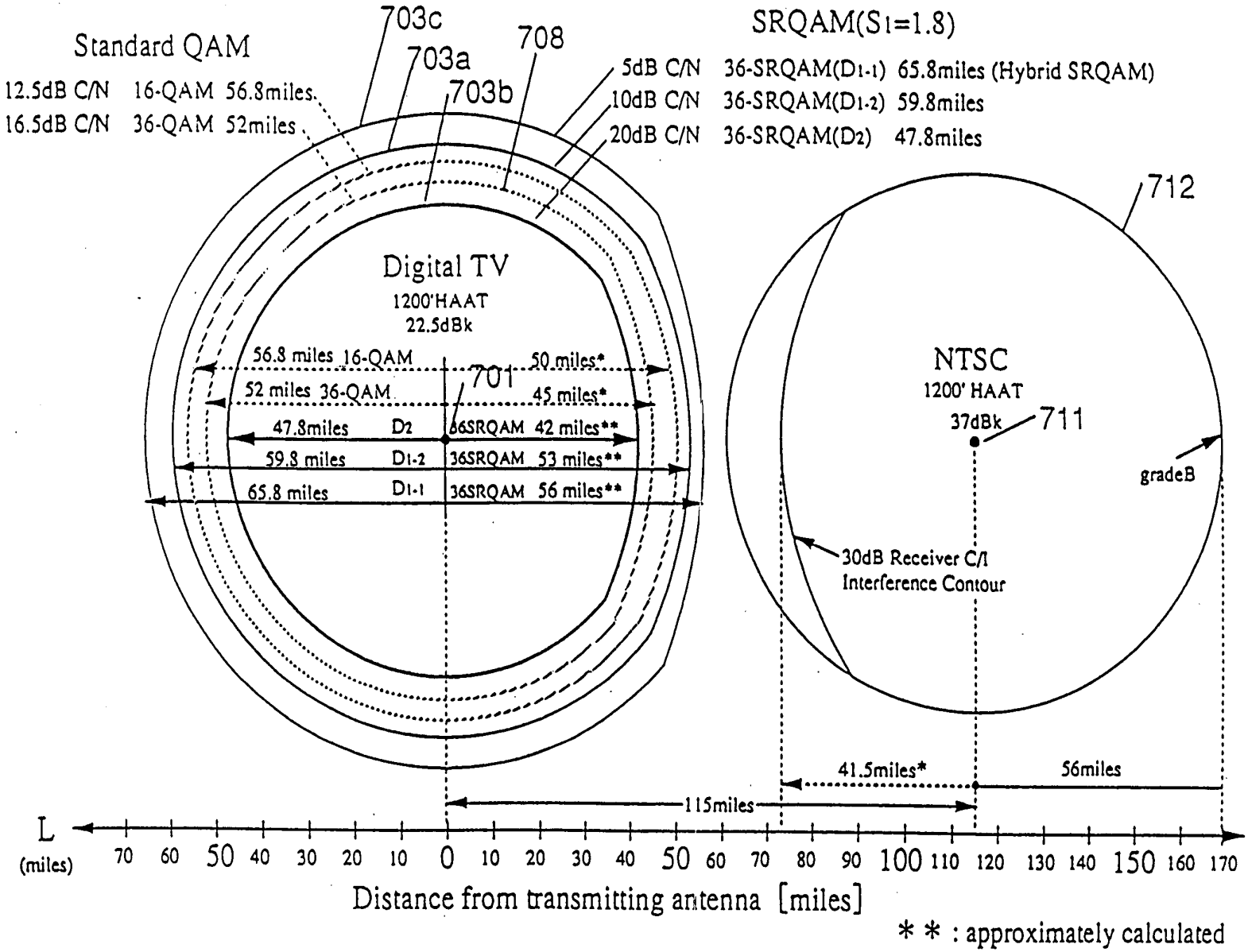

Standard QAM
12.5dB C/N 16-QAM 56.8miles
16.5dB C/N 36-QAM 52miles
703c
703a
703b
708
SRQAM(S=2.5)
2.5dB C/N 36-SRQAM(D1-1) 70.4miles (Hybrid SRQAM)
7.5dB C/N 36-SRQAM(D1-2) 62.8miles
22.5dB C/N 36-SRQAM(D2) 44.8miles
712
Digital TV
1200'HAAT
22.5dBk
56.8miles 16-QAM
50miles*
701
52miles 36-QAM
45miles*
44.8miles D2 36-SRQAM 39miles**
62.8miles D1-2 36-SRQAM 54miles**
70miles D1-1 36-SRQAM 56miles**
NTSC
1200' HAAT
37dBk
711
gradeB
30dB Receiver C/I
Interference Contour
41.5miles*
56miles
115miles
L
(miles)
70 60 50 40 30 20 10 0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170
Distance from transmitting antenna [miles]

FIG. 107



* * : approximately calculated

FIG. 108

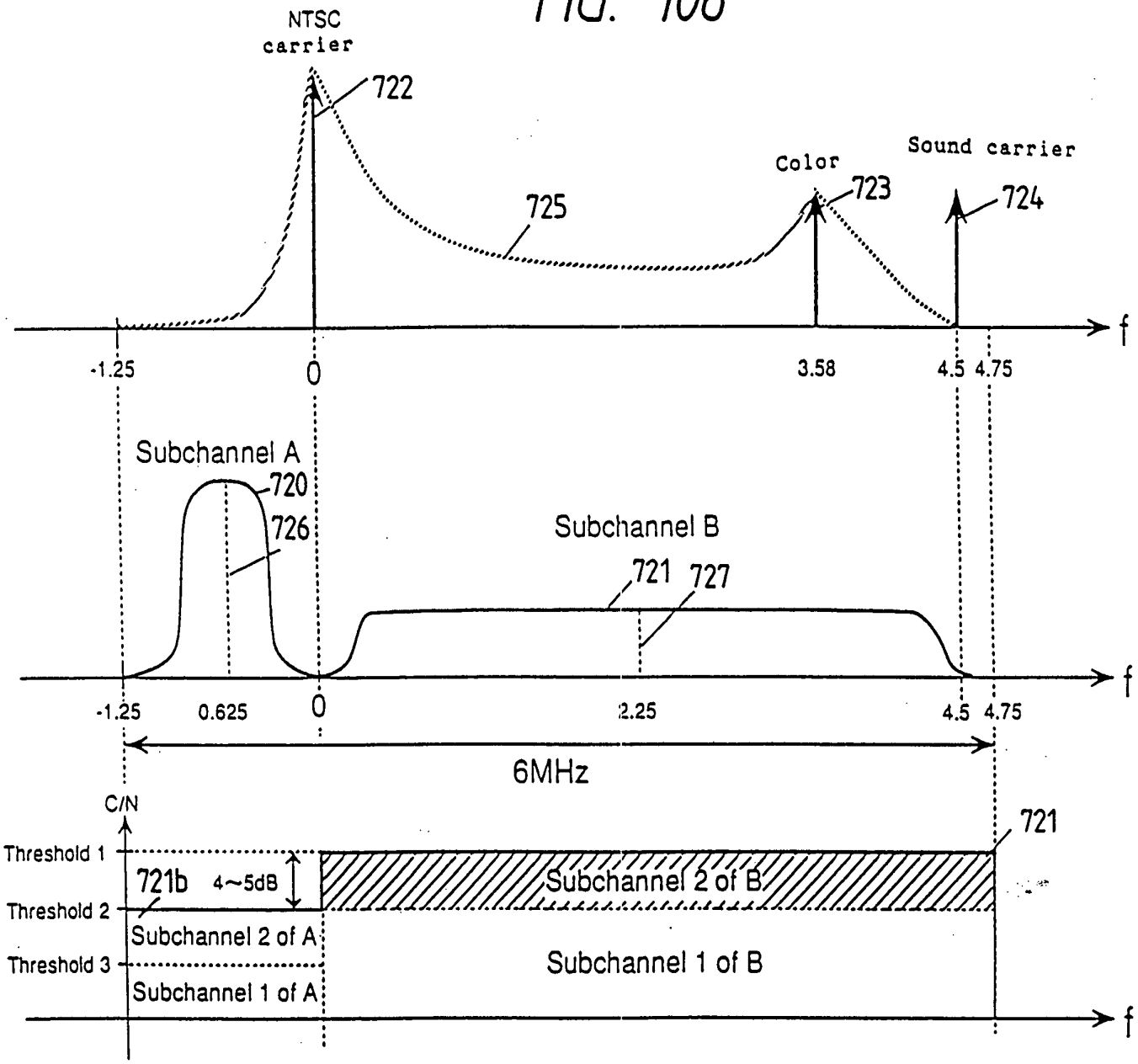

NTSC carrier
722
725
Color
723
Sound carrier
724
f
-1.25
0
3.58
4.5
4.75
Subchannel A
720
726
Subchannel B
721
727
f
-1.25
0.625
0
2.25
4.5
4.75
6MHz
C/N
721
Threshold 1
721b
4~5dB
Subchannel 2 of B
Threshold 2
Subchannel 2 of A
Threshold 3
Subchannel 1 of B
Subchannel 1 of A
f

FIG. 109

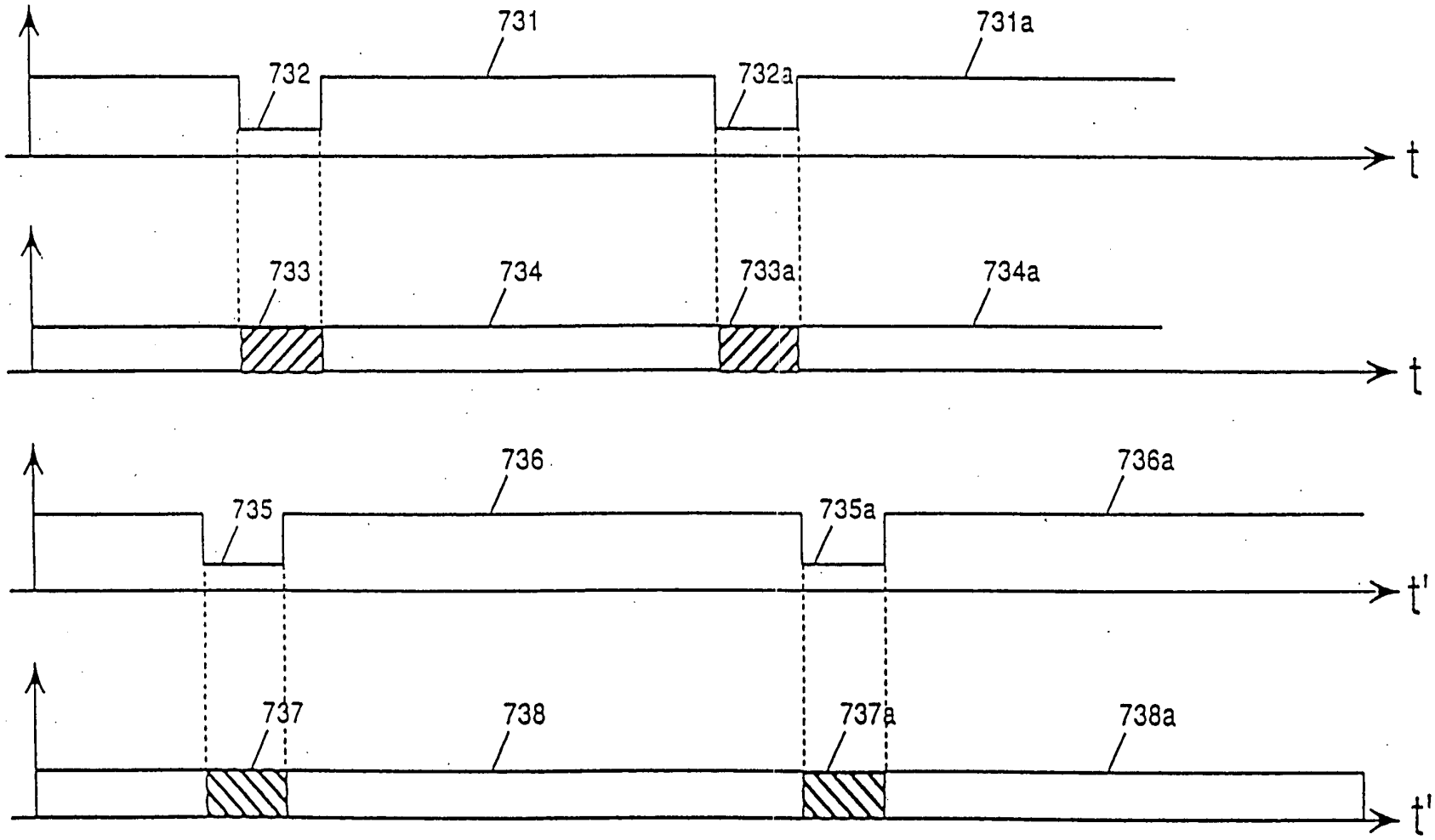

731
731a
732
732a
t
733
734
733a
734a
t
736
736a
735
735a
t'
737
738
737a
738a
t'

FIG. 110

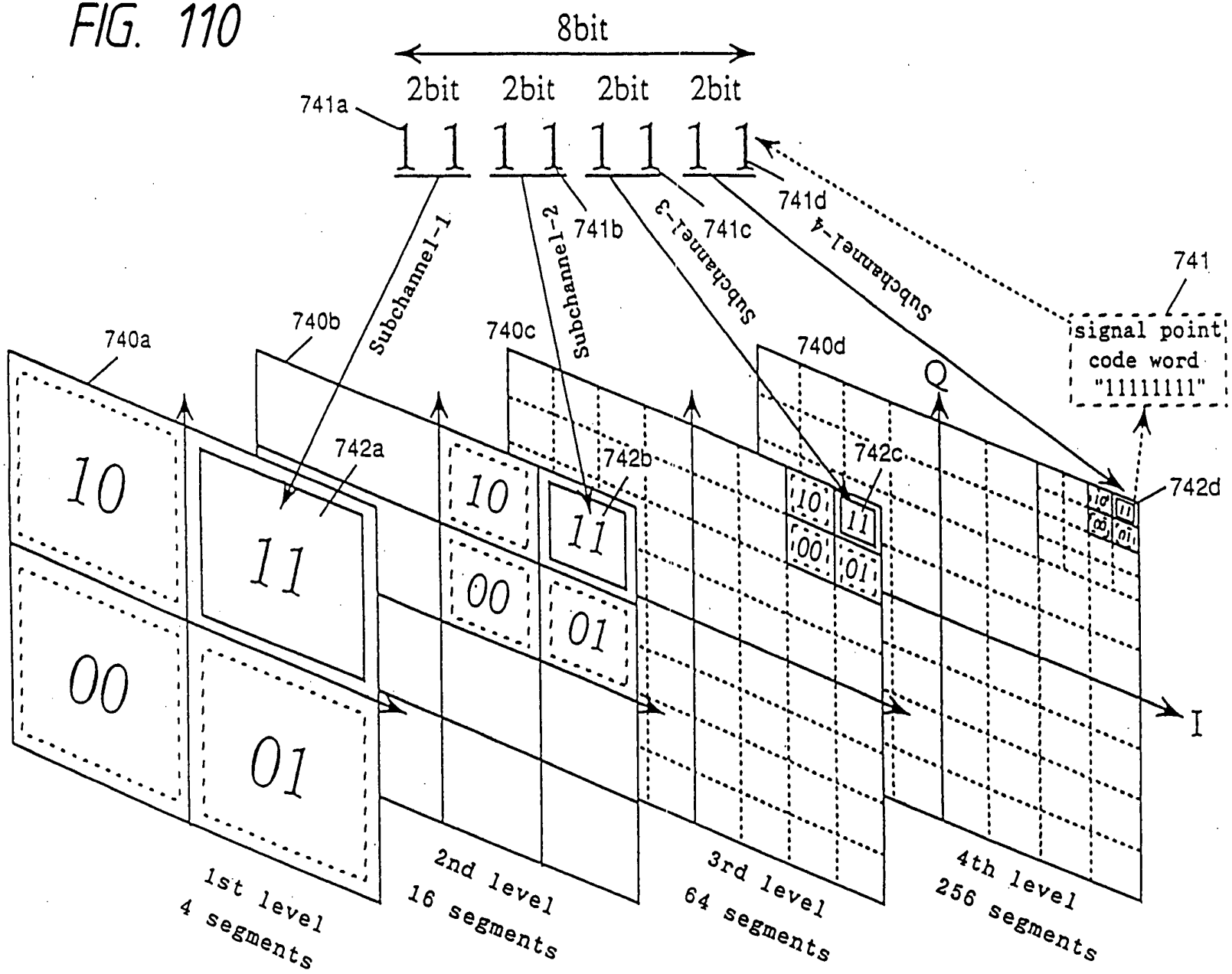

8bit
2bit 2bit 2bit 2bit
741a
1 1 1 1 1 1 1 1
741b
741c
741d
Subchannel-1
Subchannel-2
Subchannel-3
Subchannel-4
741
signal point
code word
"11111111"
740a
740b
740c
740d
Q
I
742a
742b
742c
742d
10
11
00
01
1st level
4 segments
2nd level
16 segments
3rd level
64 segments
4th level
256 segments

FIG. 111

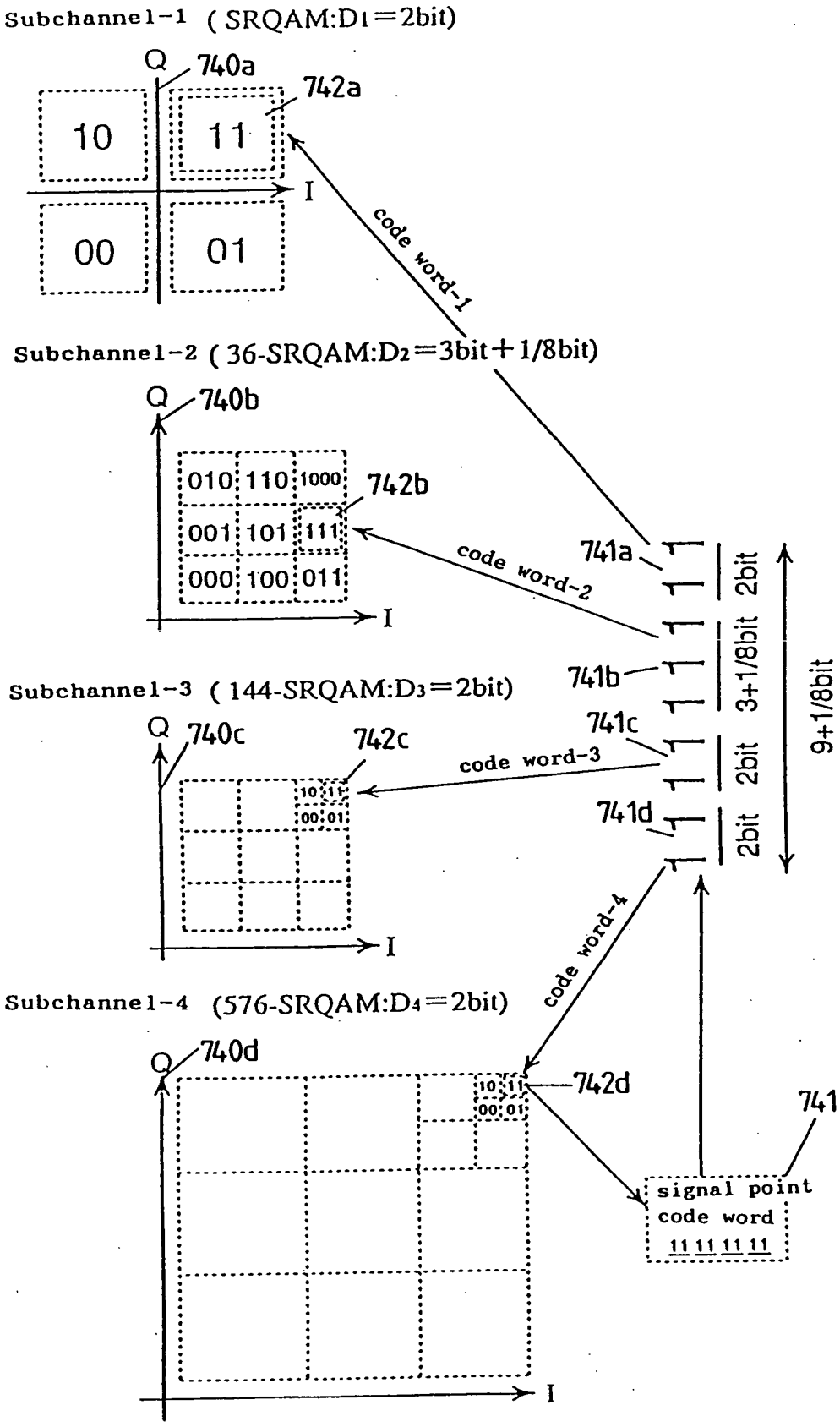

Subchannel-1 (SRQAM:D1=2bit)
Q
740a
742a
10
11
00
01
I
code word-1
Subchannel-2 (36-SRQAM:D2=3bit+1/8bit)
Q
740b
010
110
1000
742b
001
101
111
000
100
011
I
code word-2
741a
741b
741c
741d
2bit
3+1/8bit
2bit
2bit
9+1/8bit
Subchannel-3 (144-SRQAM:D3=2bit)
Q
740c
742c
code word-3
I
Subchannel-4 (576-SRQAM:D4=2bit)
code word-4
Q
740d
742d
I
741
signal point
code word
11 11 11 11

FIG. 112

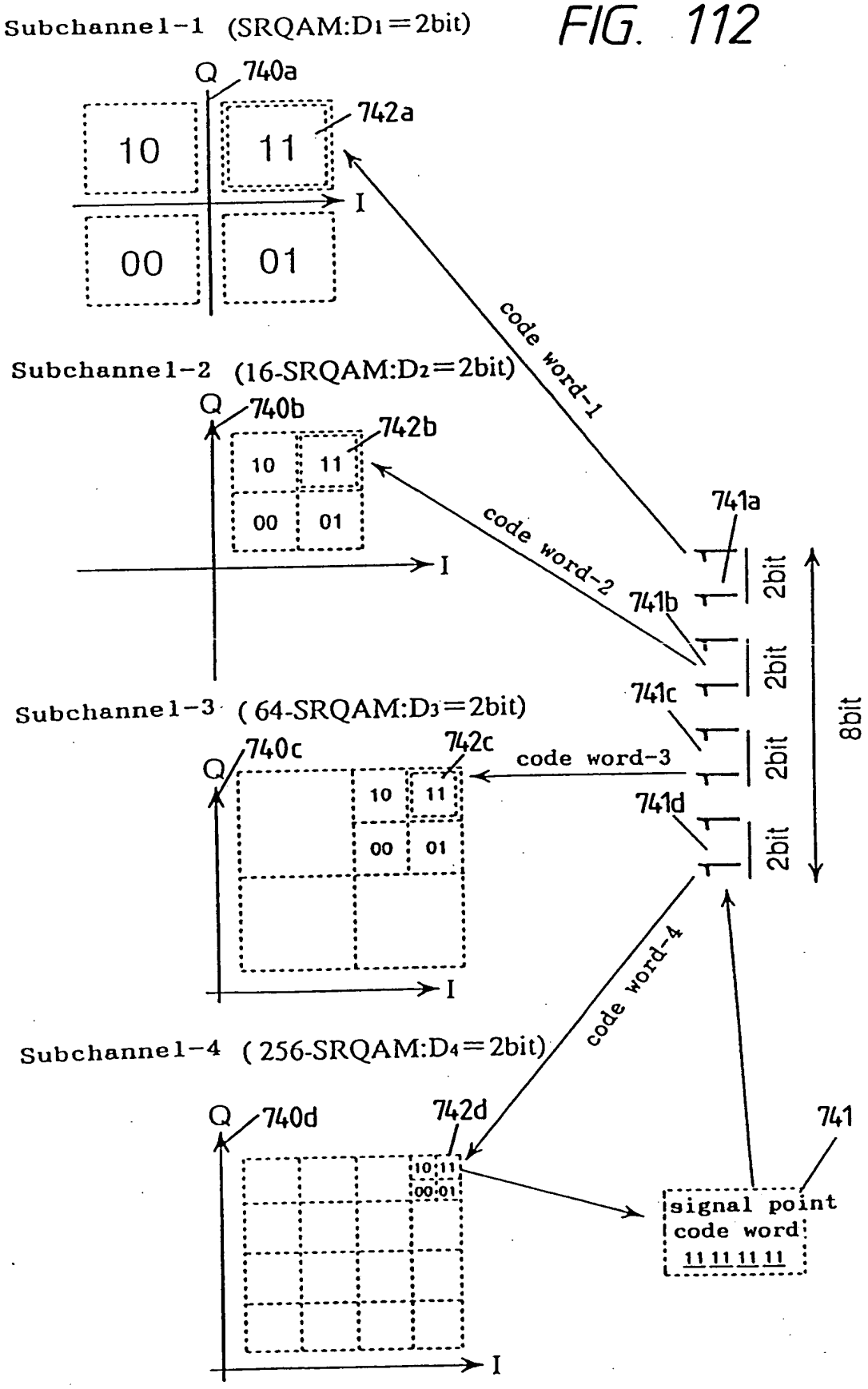

Subchannel-1 (SRQAM:D1=2bit)
Q
740a
742a
10
11
00
01
I
code word-1
Subchannel-2 (16-SRQAM:D2=2bit)
740b
742b
code word-2
Subchannel-3 (64-SRQAM:D3=2bit)
740c
742c
code word-3
Subchannel-4 (256-SRQAM:D4=2bit)
740d
742d
code word-4
741a
741b
741c
741d
2bit
8bit
741
signal point
code word
11 11 11 11

FIG. 113

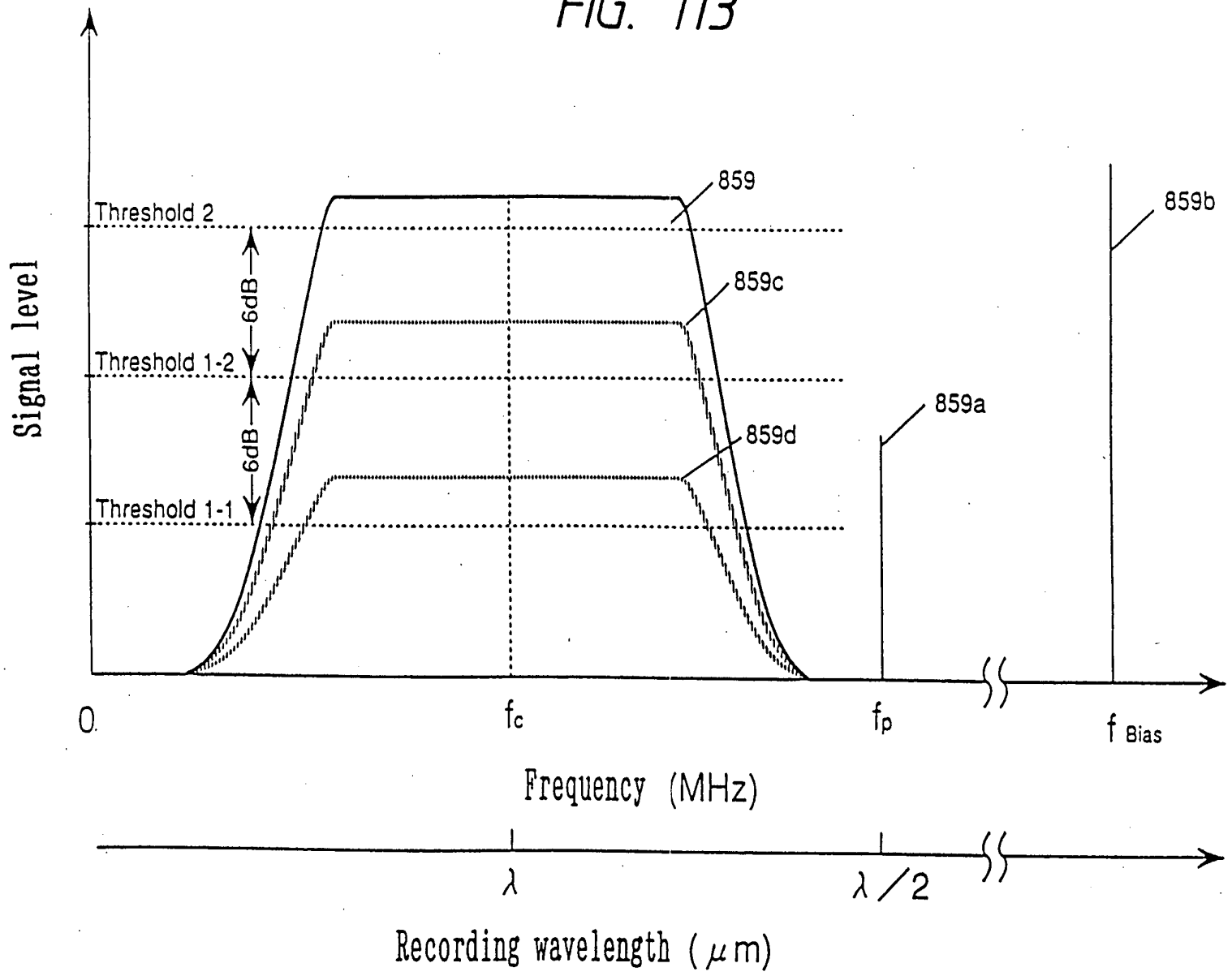

Signal level
Threshold 2
Threshold 1-2
Threshold 1-1
6dB
6dB
859
859c
859d
859a
859b
0
fc
fp
f Bias
Frequency (MHz)
λ
λ/2
Recording wavelength (μm)

FIG. 114

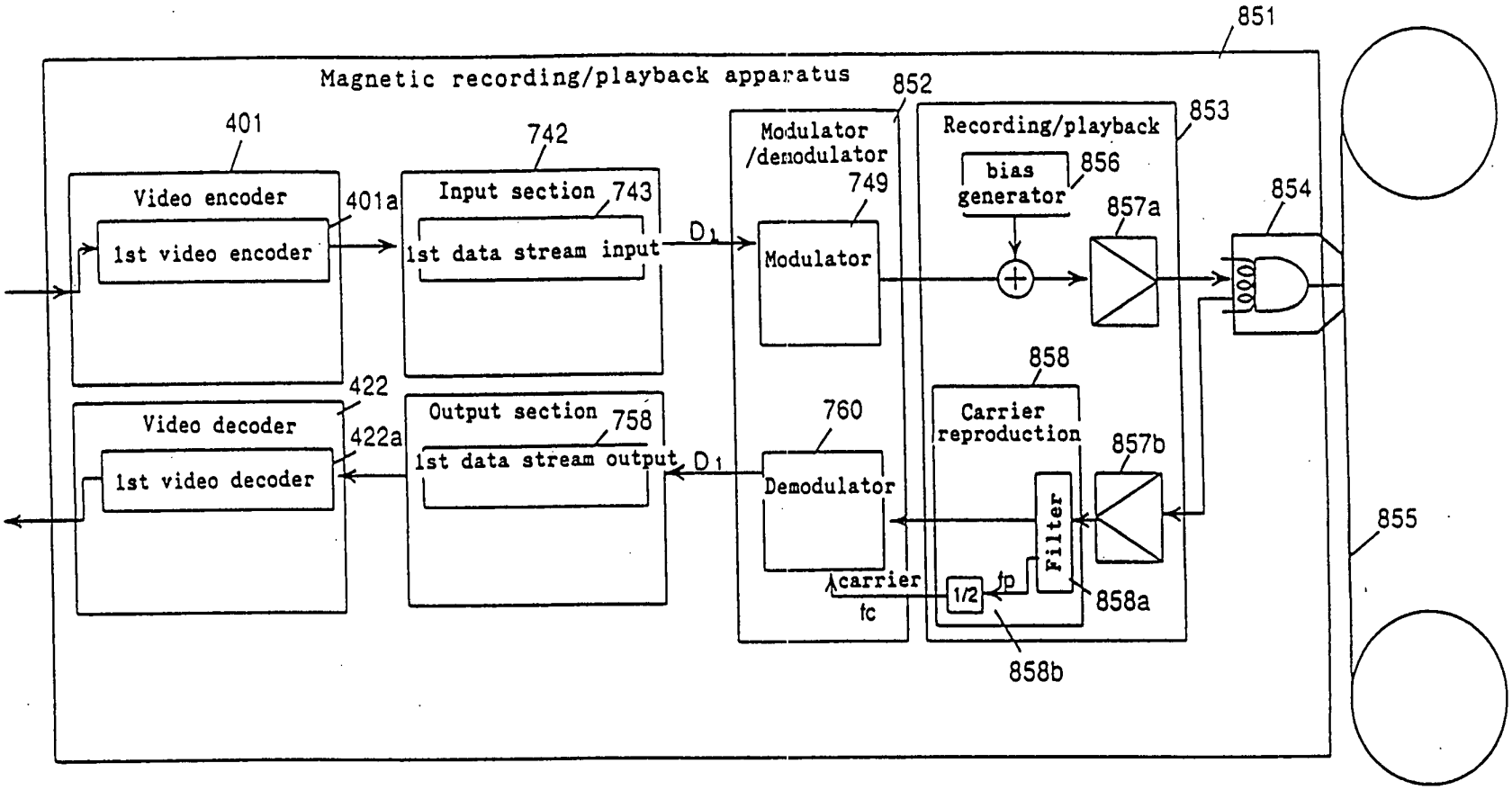

851
Magnetic recording/playback apparatus
852
401
742
Modulator /demodulator
853
Recording/playback
bias generator
856
854
Video encoder
401a
Input section
743
749
857a
1st video encoder
1st data stream input
D1
Modulator
858
422
Output section
758
760
Carrier reproduction
857b
Video decoder
422a
1st data stream output
D1
Demodulator
Filter
855
carrier
fc
1/2
fp
858a
858b

FIG. 115

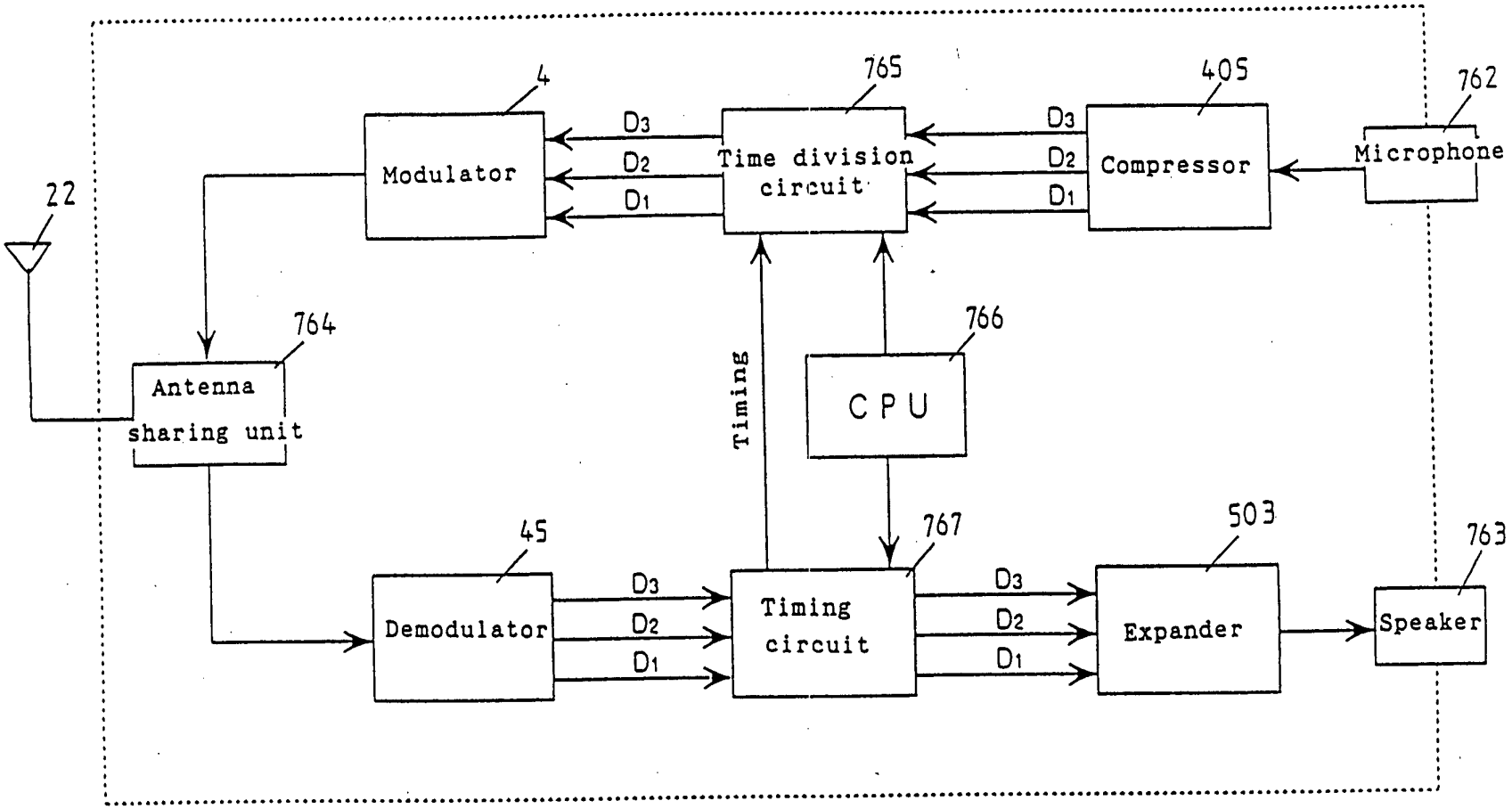

22
4
765
405
762
Modulator
D3
D2
D1
Time division circuit
Compressor
Microphone
764
Antenna sharing unit
Timing
766
CPU
45
767
503
763
Demodulator
Timing circuit
Expander
Speaker

FIG. 116

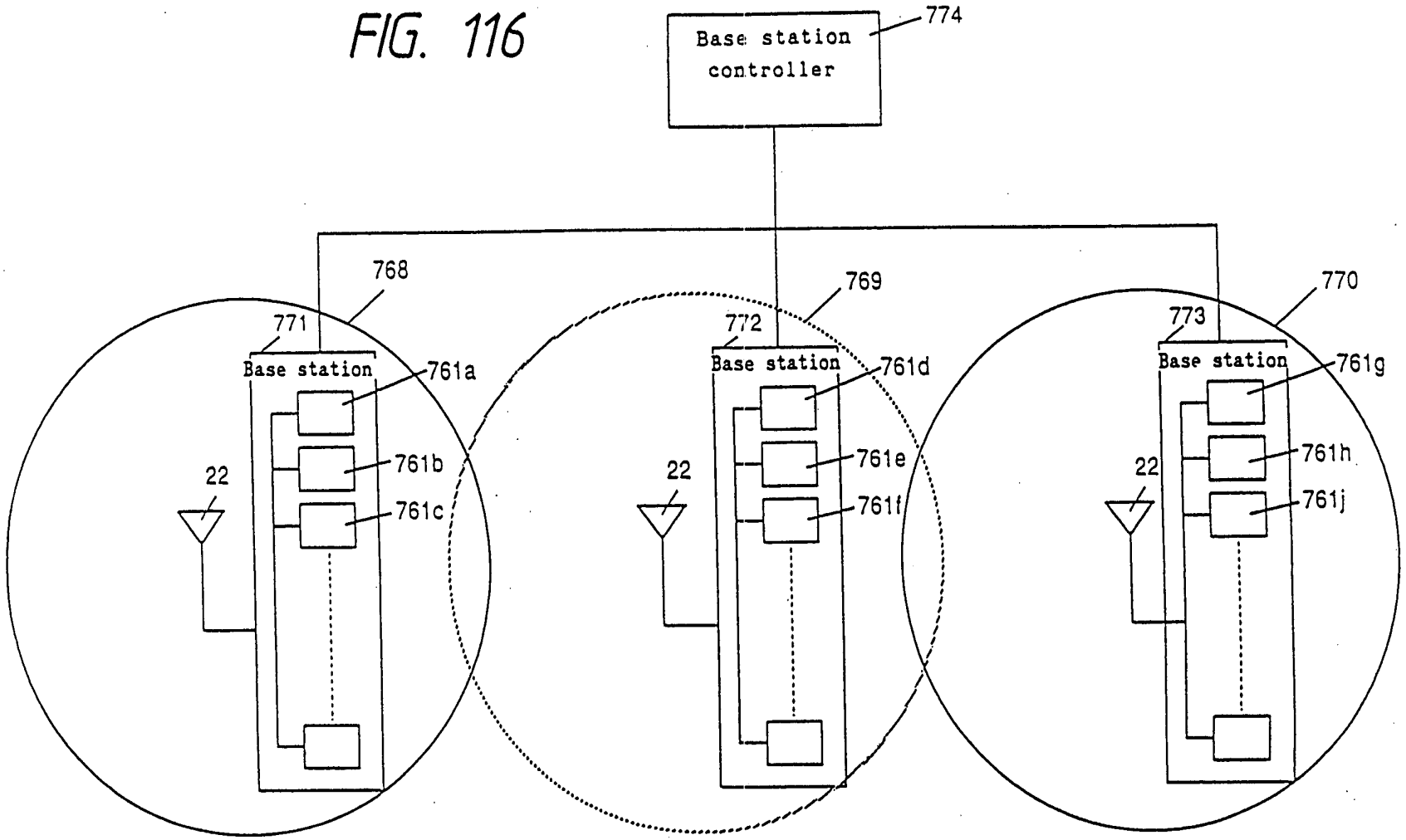

Base station controller
774
768
769
770
771
772
773
Base station
Base station
Base station
761a
761b
761c
761d
761e
761f
761g
761h
761j
22
22
22

FIG. 117

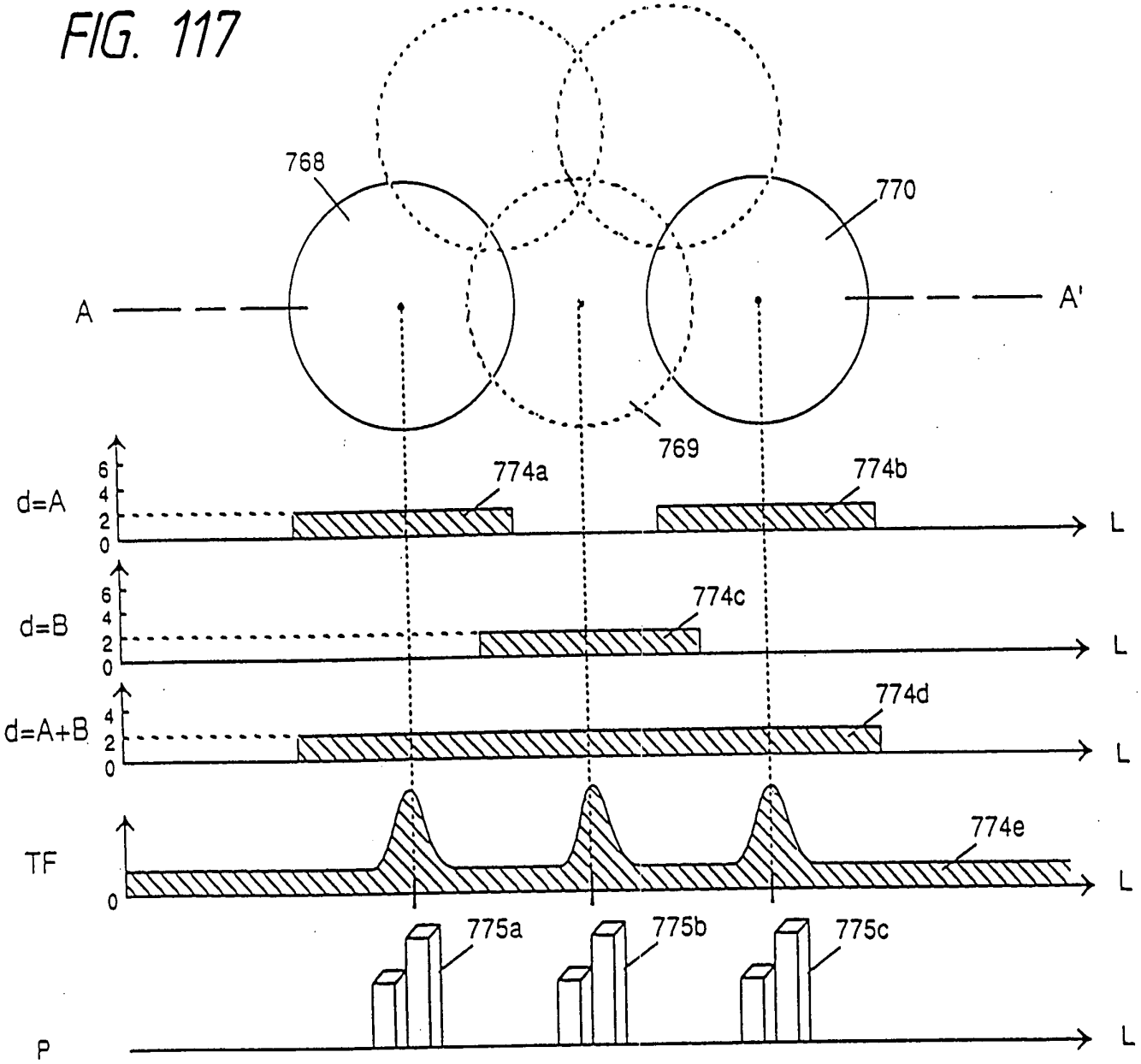

768
770
A
A'
769
d=A
6
4
2
0
774a
774b
L
d=B
774c
d=A+B
774d
TF
774e
775a
775b
775c
P

FIG. 118

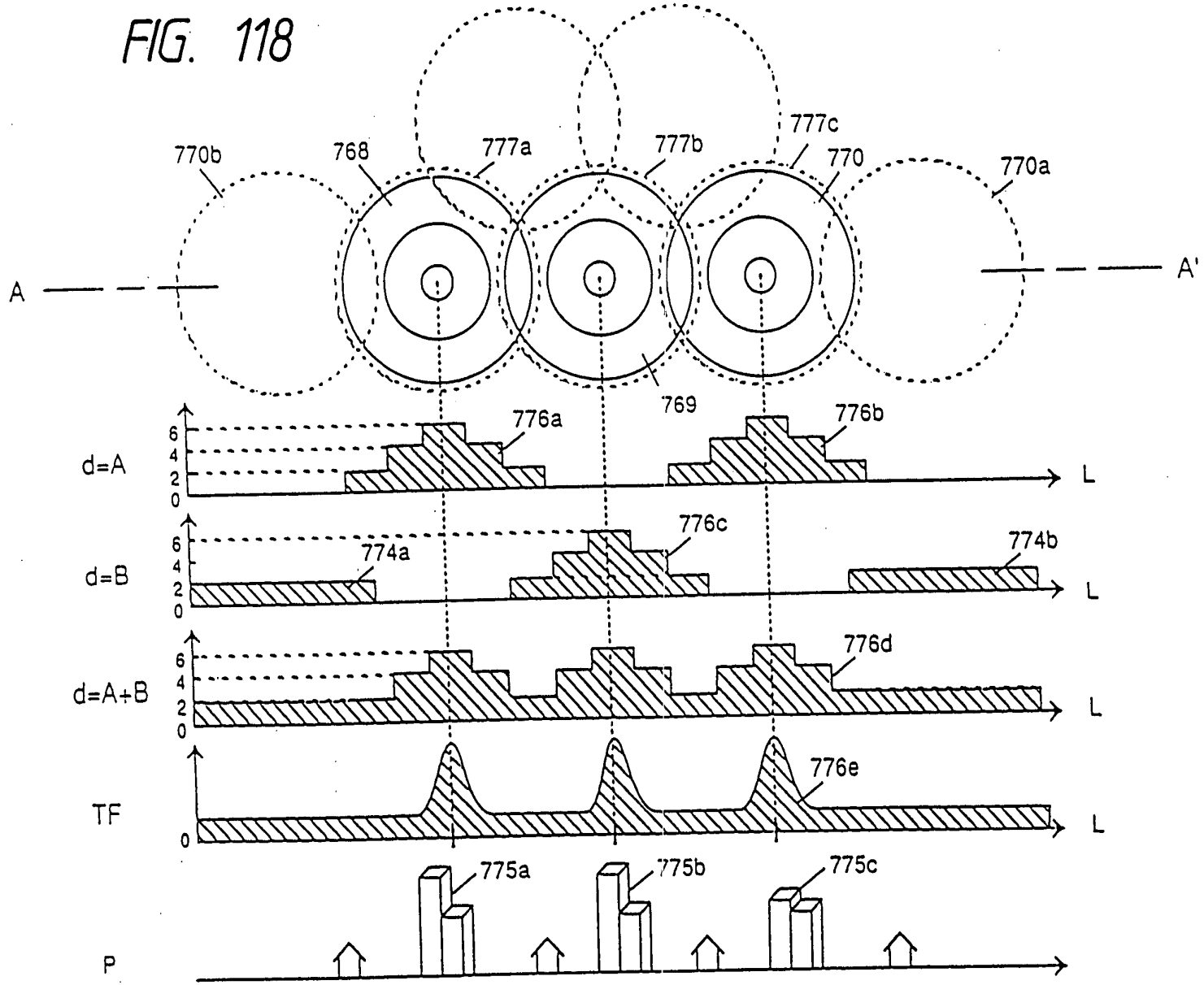

770b
768
777a
777b
777c
770
770a
A
A'
769
776a
776b
d=A
6
4
2
0
L
776c
774a
774b
d=B
776d
d=A+B
776e
TF
775a
775b
775c
P

FIG. 119

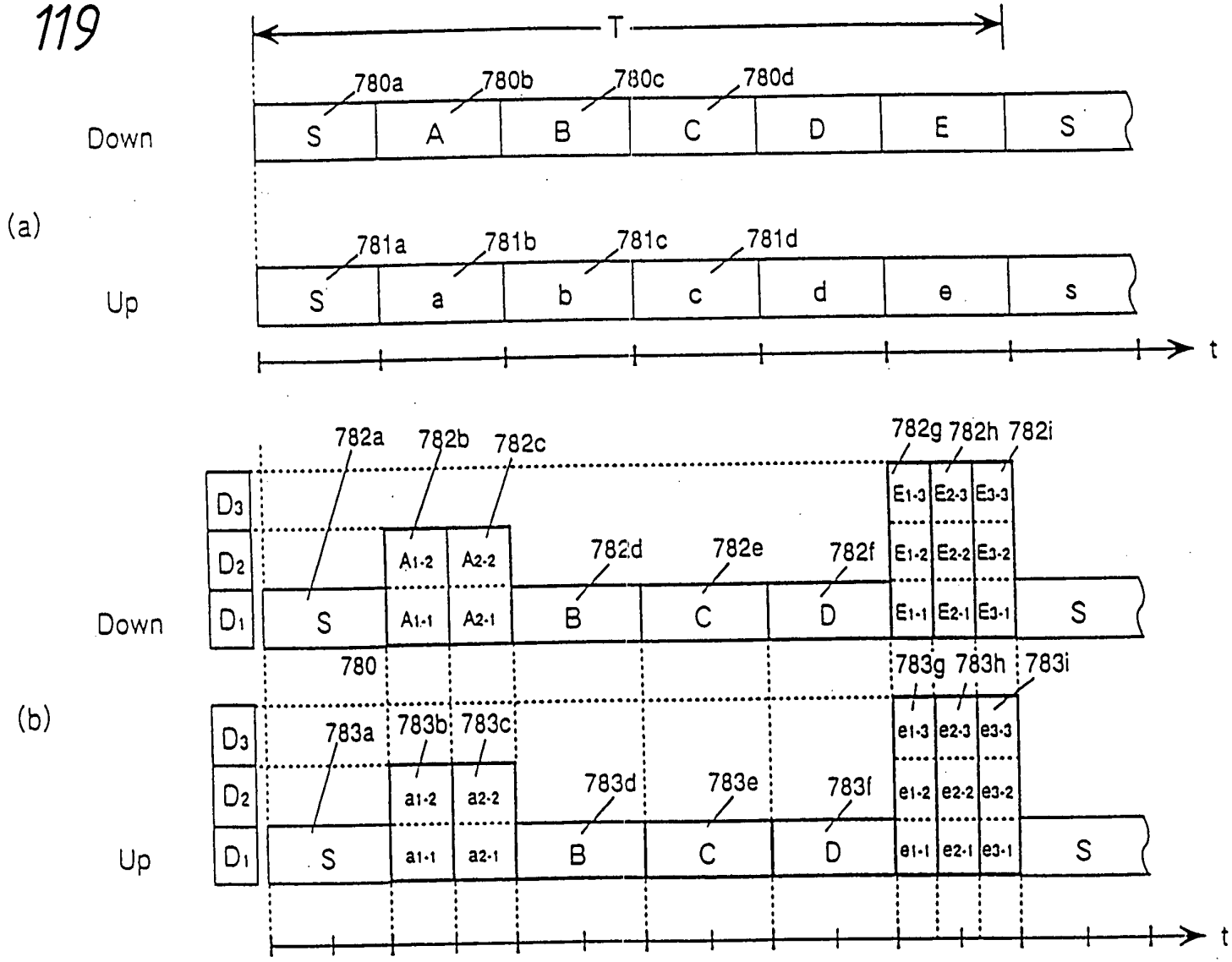

T
780a
780b
780c
780d
Down
S
A
B
C
D
E
S
(a)
781a
781b
781c
781d
Up
S
a
b
c
d
e
s
t
782a
782b
782c
782g
782h
782i
D3
D2
D1
A1-2
A2-2
782d
782e
782f
E1-3
E2-3
E3-3
E1-2
E2-2
E3-2
Down
S
A1-1
A2-1
B
C
D
E1-1
E2-1
E3-1
S
780
783g
783h
783i
(b)
783a
783b
783c
e1-3
e2-3
e3-3
a1-2
a2-2
783d
783e
783f
e1-2
e2-2
e3-2
Up
S
a1-1
a2-1
B
C
D
e1-1
e2-1
e3-1
S
t

FIG. 120

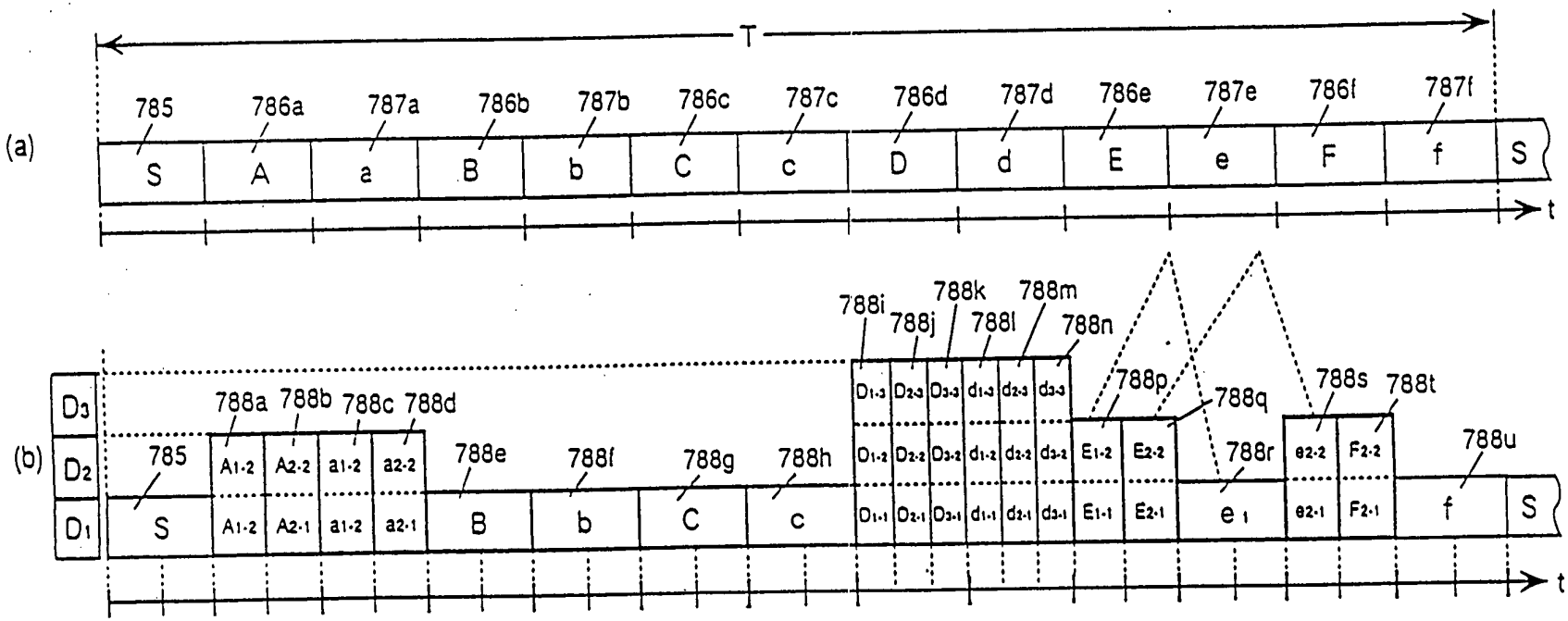

(a)
T
785
786a
787a
786b
787b
786c
787c
786d
787d
786e
787e
786f
787f
S
A
a
B
b
C
c
D
d
E
e
F
f
S
t
(b)
D3
D2
D1
788i
788j
788k
788l
788m
788n
788p
788q
788r
788s
788t
788u
788a
788b
788c
788d
788e
788f
788g
788h
785
S
B
b
C
c
e1
f
S
t

FIG. 121

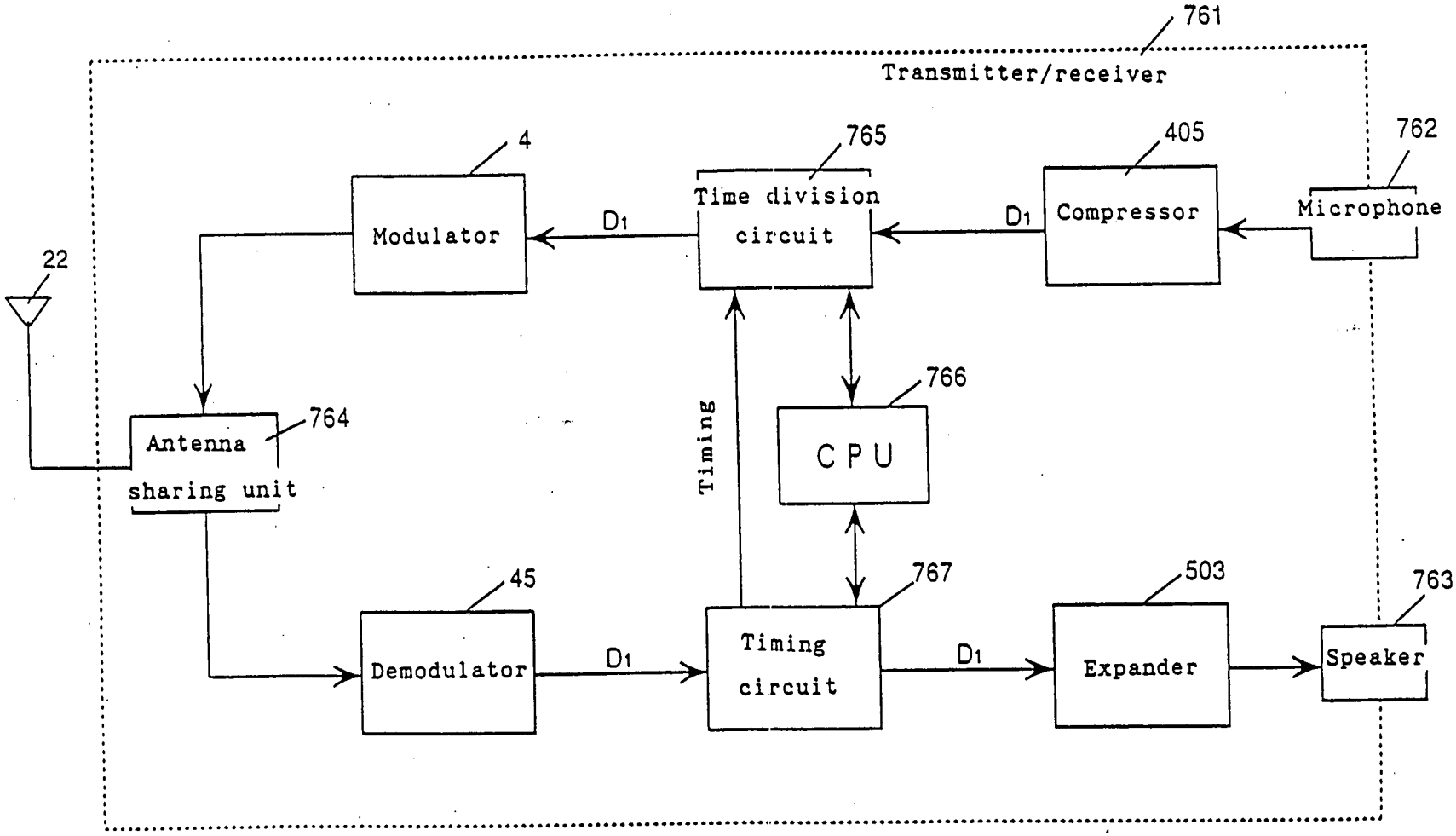

761
Transmitter/receiver
4
765
405
762
Modulator
D1
Time division circuit
D1
Compressor
Microphone
22
766
764
Antenna sharing unit
Timing
C P U
45
767
503
763
Demodulator
D1
Timing circuit
D1
Expander
Speaker

FIG. 122

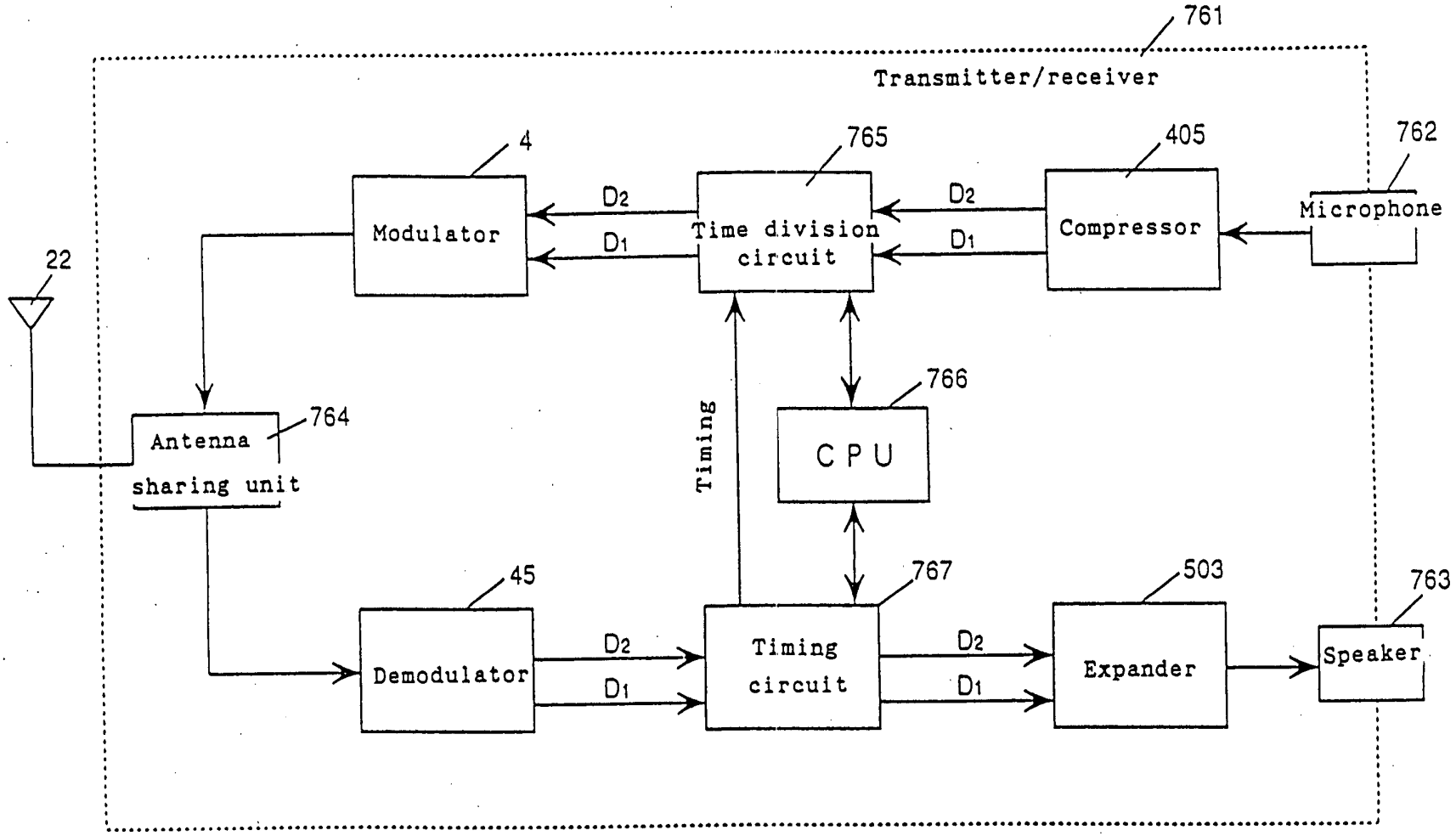

761
Transmitter/receiver
4
765
405
762
Modulator
D2
D1
Time division circuit
D2
D1
Compressor
Microphone
22
Antenna sharing unit
764
Timing
766
CPU
45
767
503
763
Demodulator
D2
D1
Timing circuit
D2
D1
Expander
Speaker

FIG. 123

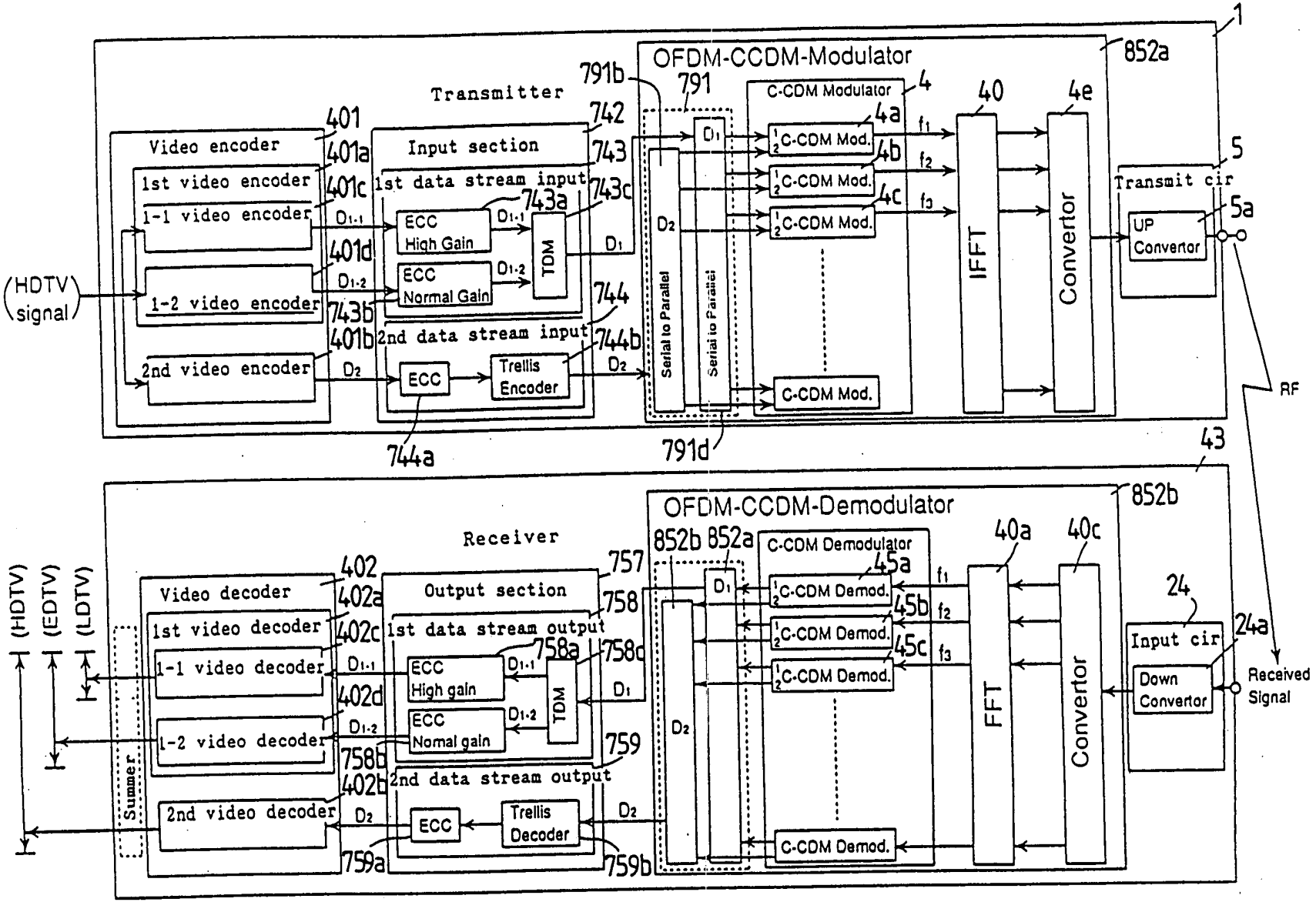

Transmitter
OFDM-CCDM-Modulator
Video encoder
1st video encoder
1-1 video encoder
1-2 video encoder
2nd video encoder
Input section
1st data stream input
2nd data stream input
ECC High Gain
ECC Normal Gain
ECC
TDM
Trellis Encoder
C-CDM Modulator
C-CDM Mod.
Serial to Parallel
IFFT
Convertor
Transmit cir
UP Convertor
(HDTV signal)
RF
Receiver
OFDM-CCDM-Demodulator
Video decoder
1st video decoder
1-1 video decoder
1-2 video decoder
2nd video decoder
Output section
1st data stream output
2nd data stream output
ECC High gain
ECC Nomal gain
ECC
TDM
Trellis Decoder
C-CDM Demodulator
C-CDM Demod.
Parallel to Serial
FFT
Convertor
Input cir
Down Convertor
Summer
(HDTV)
(EDTV)
(LDTV)
Received Signal

FIG. 124

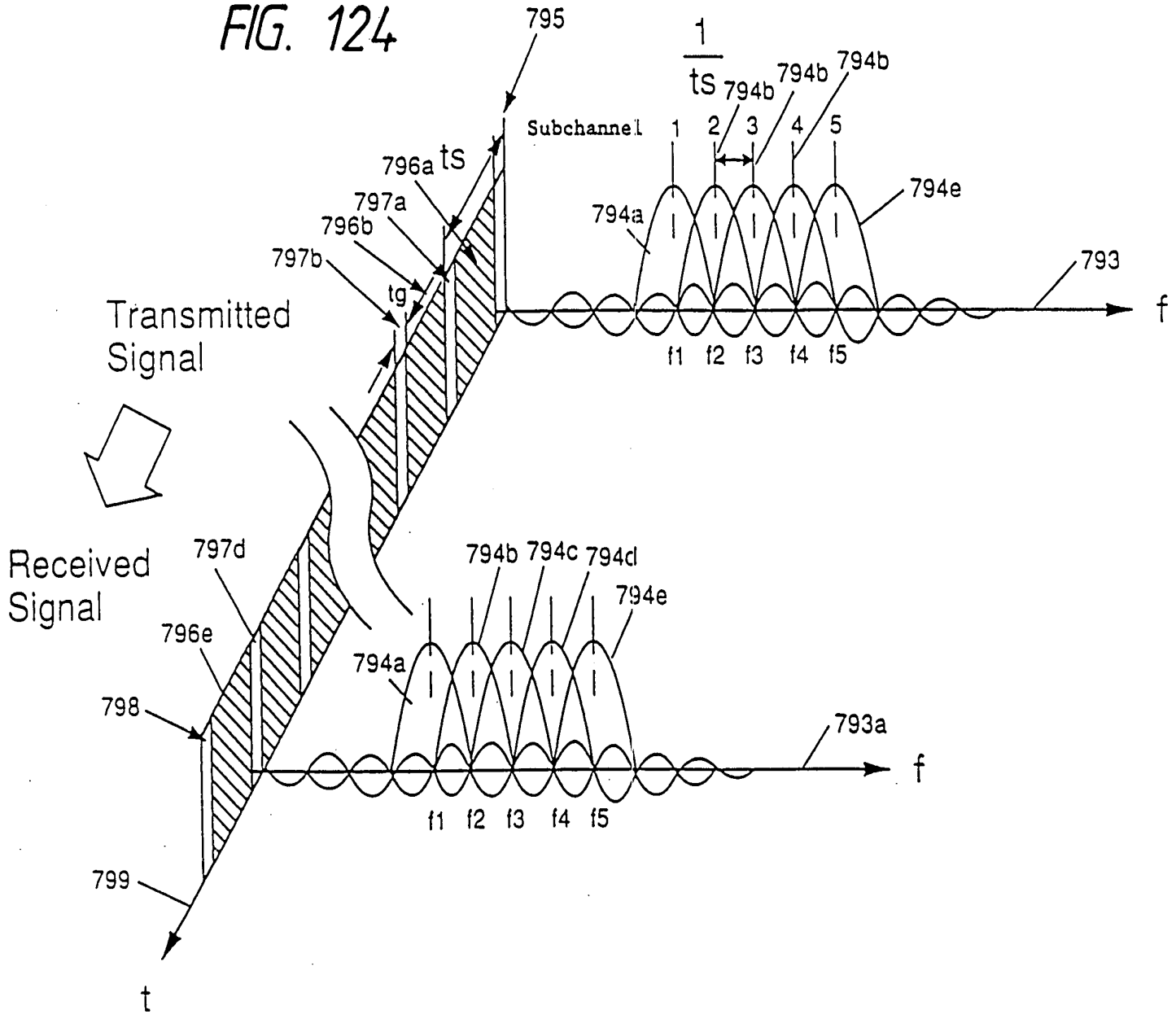

795
1/tS
794b
794b
794b
Subchannel
1
2
3
4
5
796a
tS
797a
796b
797b
tg
794a
794e
793
f
Transmitted Signal
f1
f2
f3
f4
f5
Received Signal
797d
794b
794c
794d
794e
796e
794a
798
793a
f
f1
f2
f3
f4
f5
799
t

FIG. 125

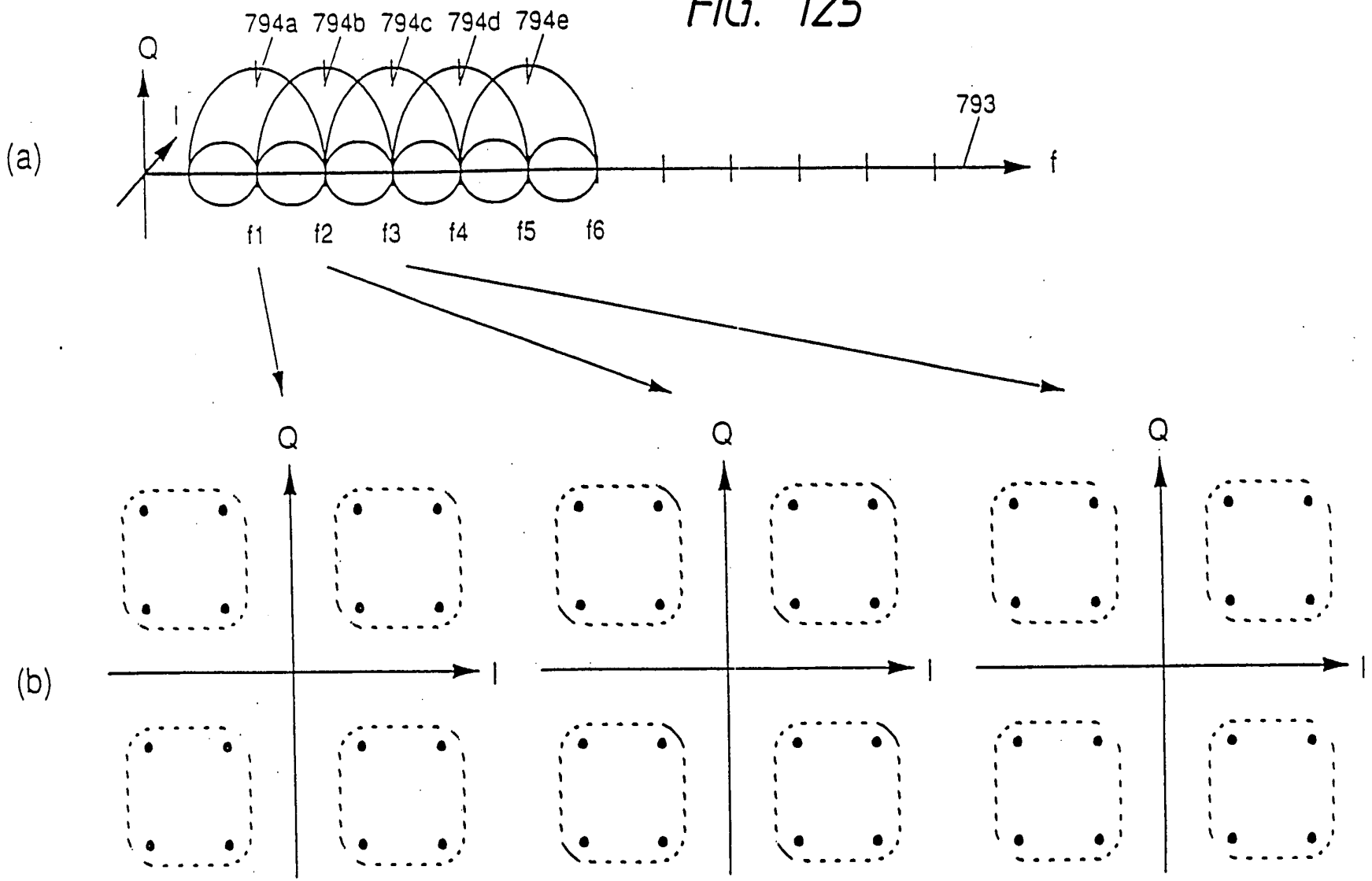


FIG. 126

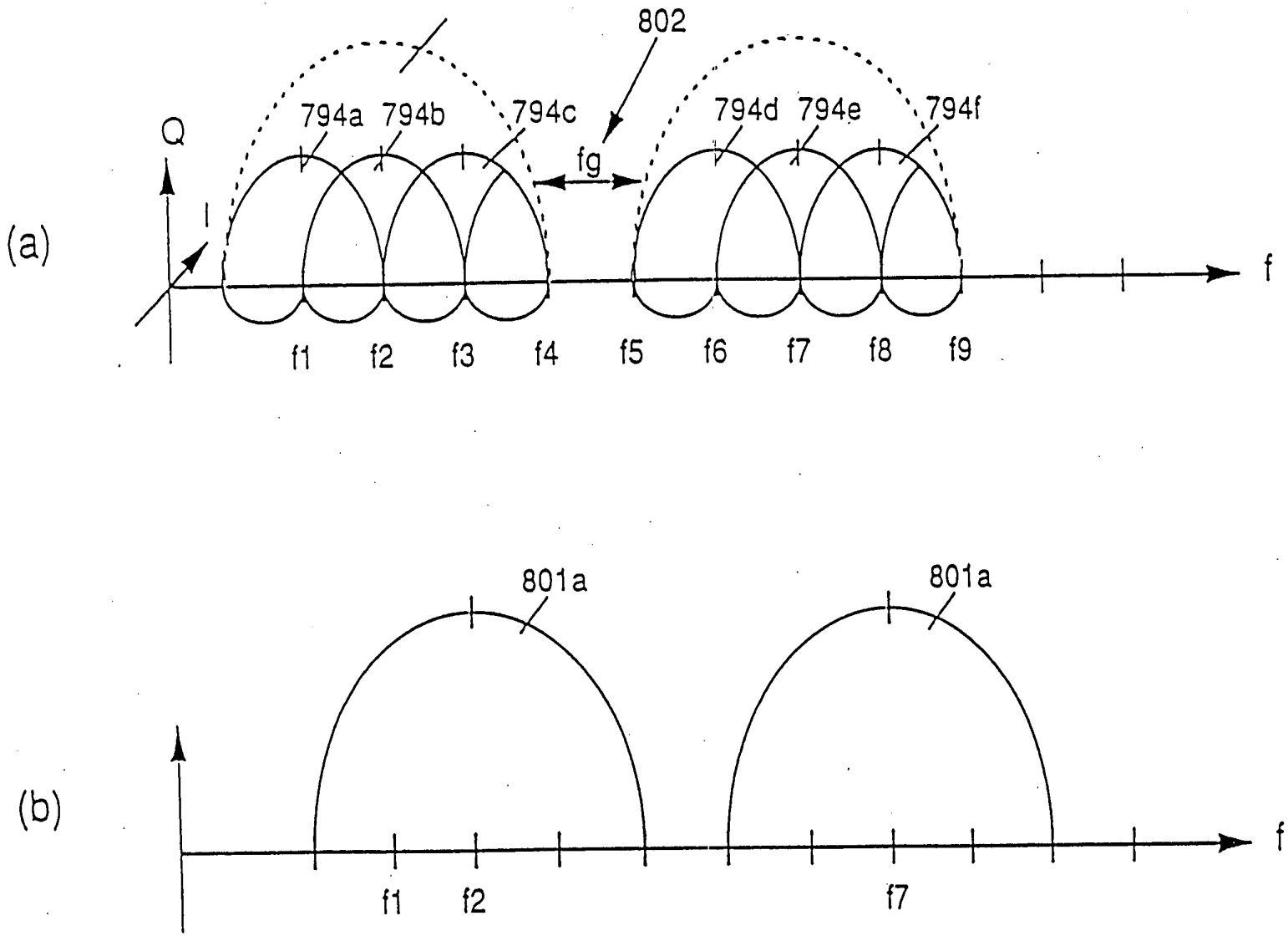

(a)
802
794a
794b
794c
794d
794e
794f
Q
I
fg
f
f1
f2
f3
f4
f5
f6
f7
f8
f9
(b)
801a
801a
f
f1
f2
f7

FIG. 127

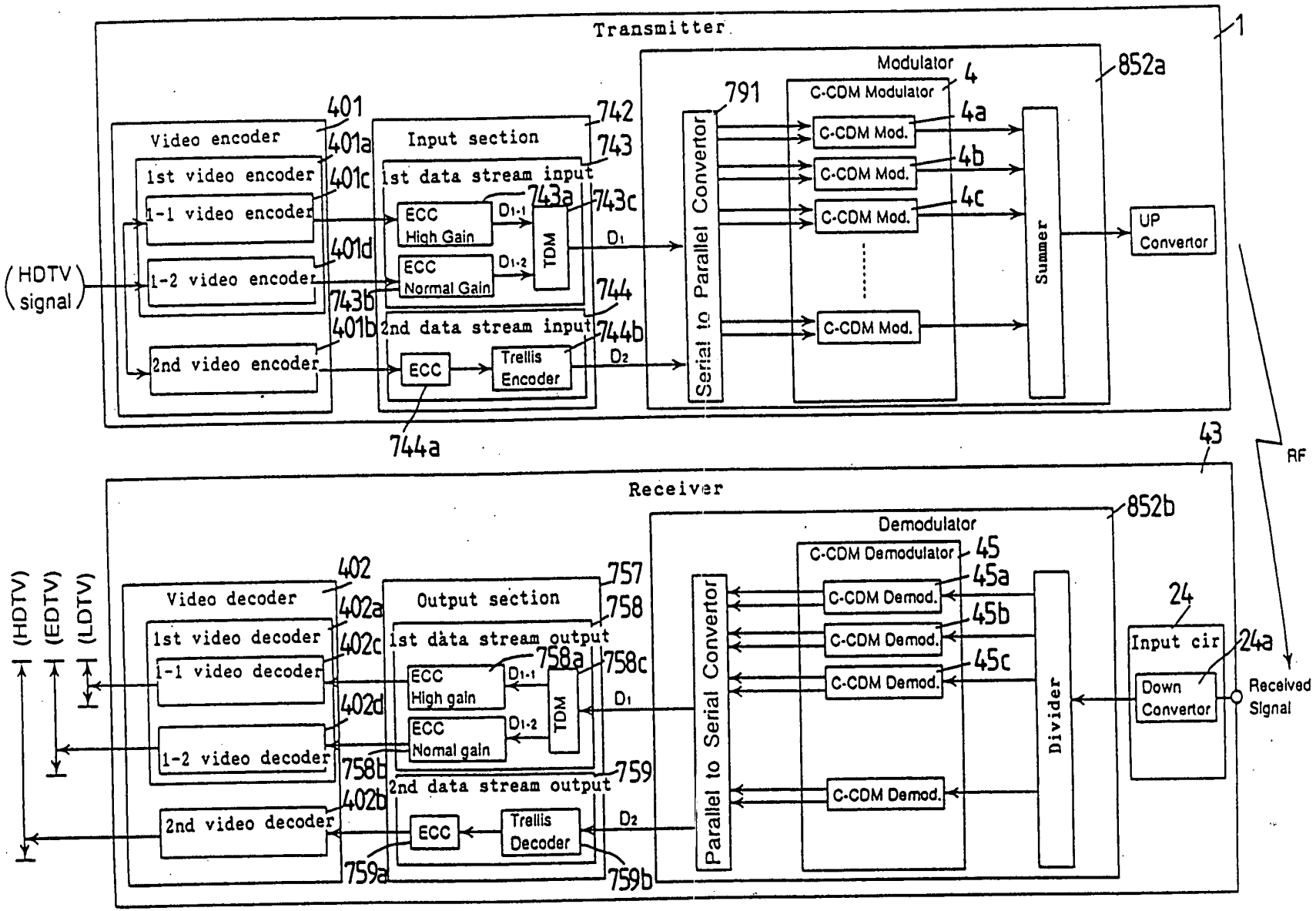

Transmitter
1
Modulator
852a
4
C-CDM Modulator
4a
4b
4c
C-CDM Mod.
C-CDM Mod.
C-CDM Mod.
C-CDM Mod.
Summer
UP Convertor
791
Serial to Parallel Convertor
401
Video encoder
401a
1st video encoder
401c
1-1 video encoder
401d
1-2 video encoder
401b
2nd video encoder
742
Input section
743
1st data stream input
743a
743c
ECC High Gain
ECC Normal Gain
D1-1
D1-2
TDM
D1
743b
744
2nd data stream input
744b
ECC
Trellis Encoder
D2
744a
(HDTV signal)
43
RF
Receiver
852b
Demodulator
C-CDM Demodulator
45
45a
45b
45c
C-CDM Demod.
C-CDM Demod.
C-CDM Demod.
C-CDM Demod.
Divider
Parallel to Serial Convertor
24
Input cir
24a
Down Convertor
Received Signal
402
Video decoder
402a
1st video decoder
402c
1-1 video decoder
402d
1-2 video decoder
402b
2nd video decoder
757
Output section
758
1st data stream output
758a
758c
ECC High gain
ECC Nomal gain
D1-1
D1-2
TDM
D1
758b
759
2nd data stream output
ECC
Trellis Decoder
D2
759a
759b
(HDTV)
(EDTV)
(LDTV)

FIG. 128

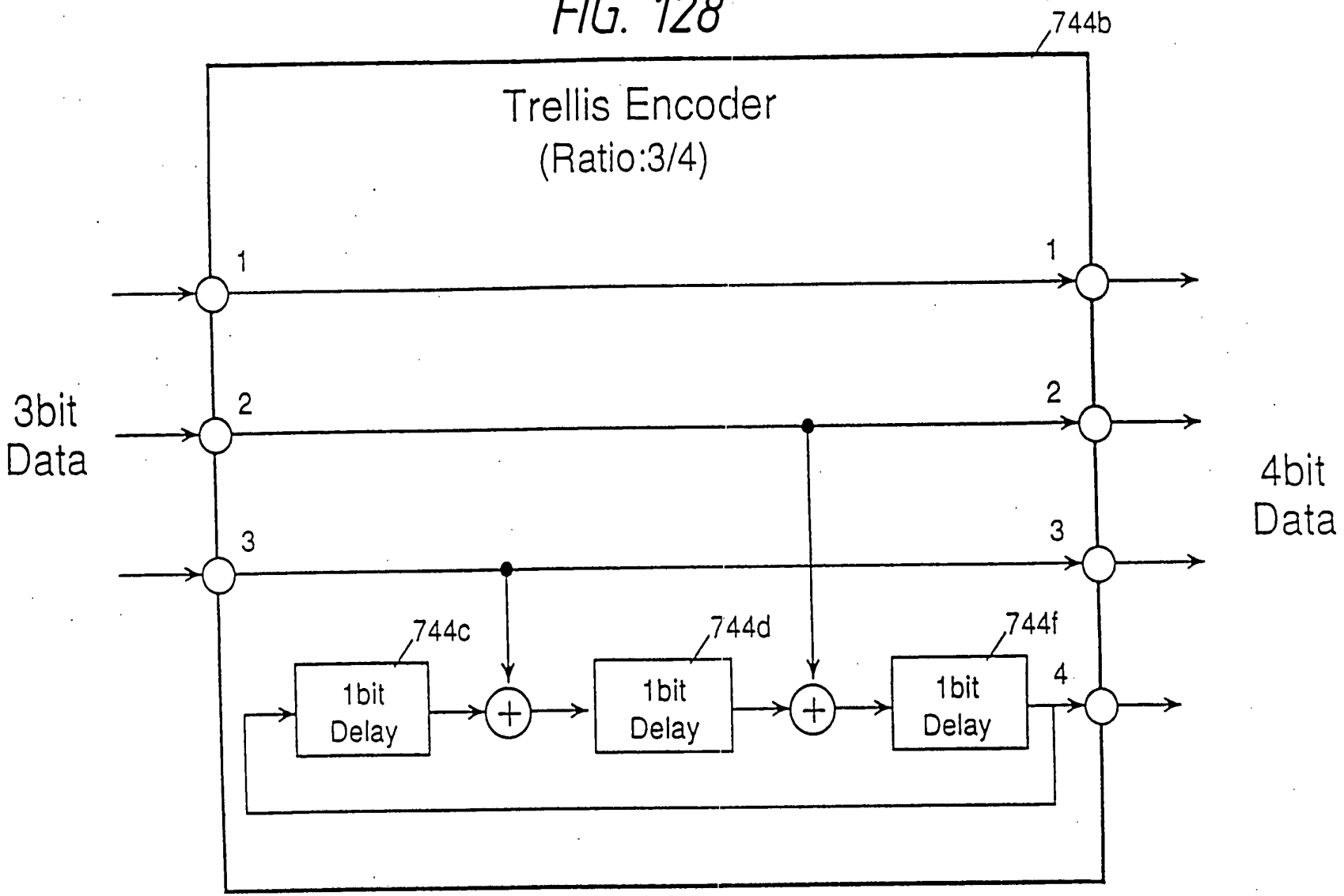

744b
Trellis Encoder
(Ratio:3/4)
3bit
Data
1
2
3
1
2
3
4
4bit
Data
744c
744d
744f
1bit
Delay
1bit
Delay
1bit
Delay

FIG. 129

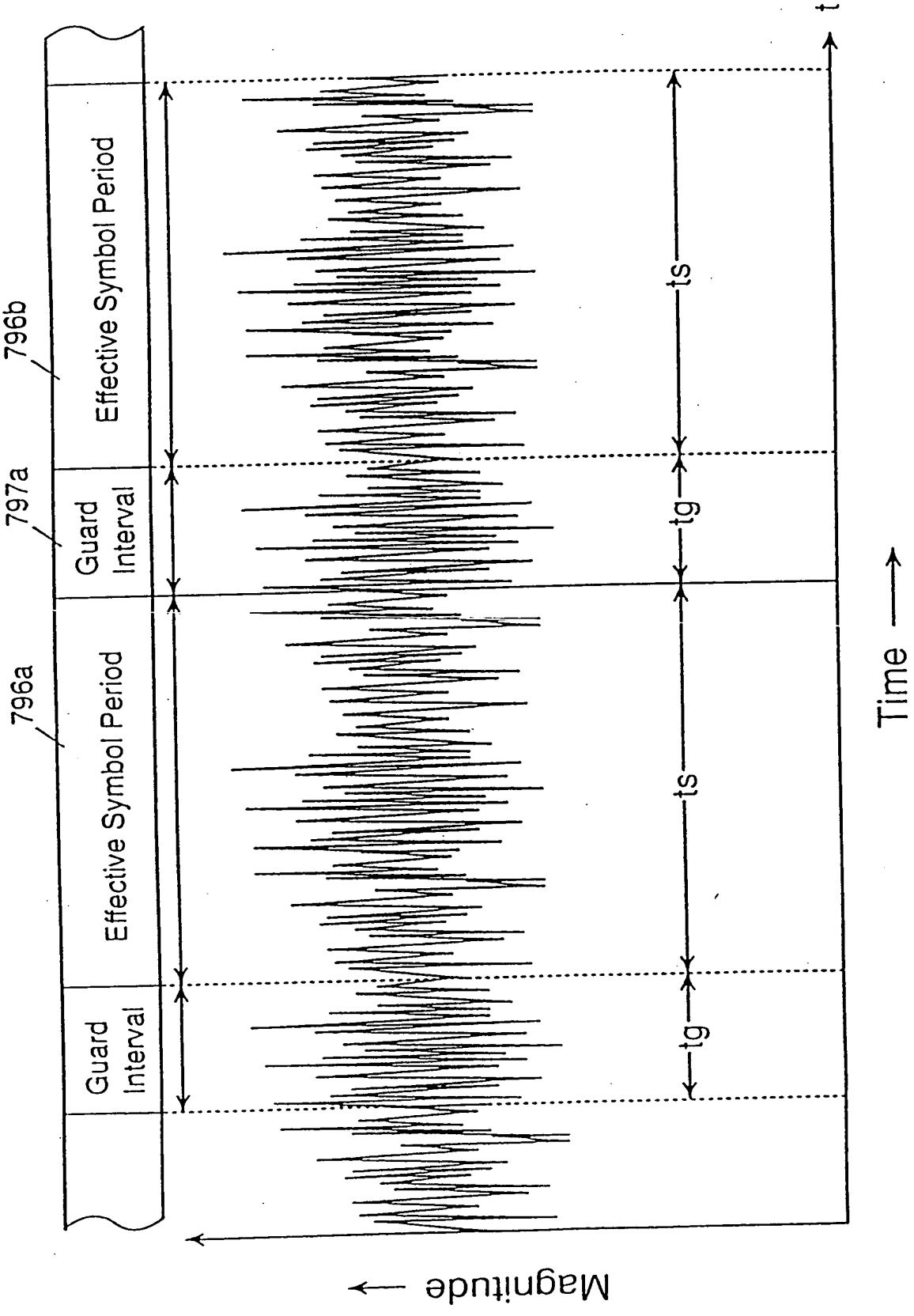
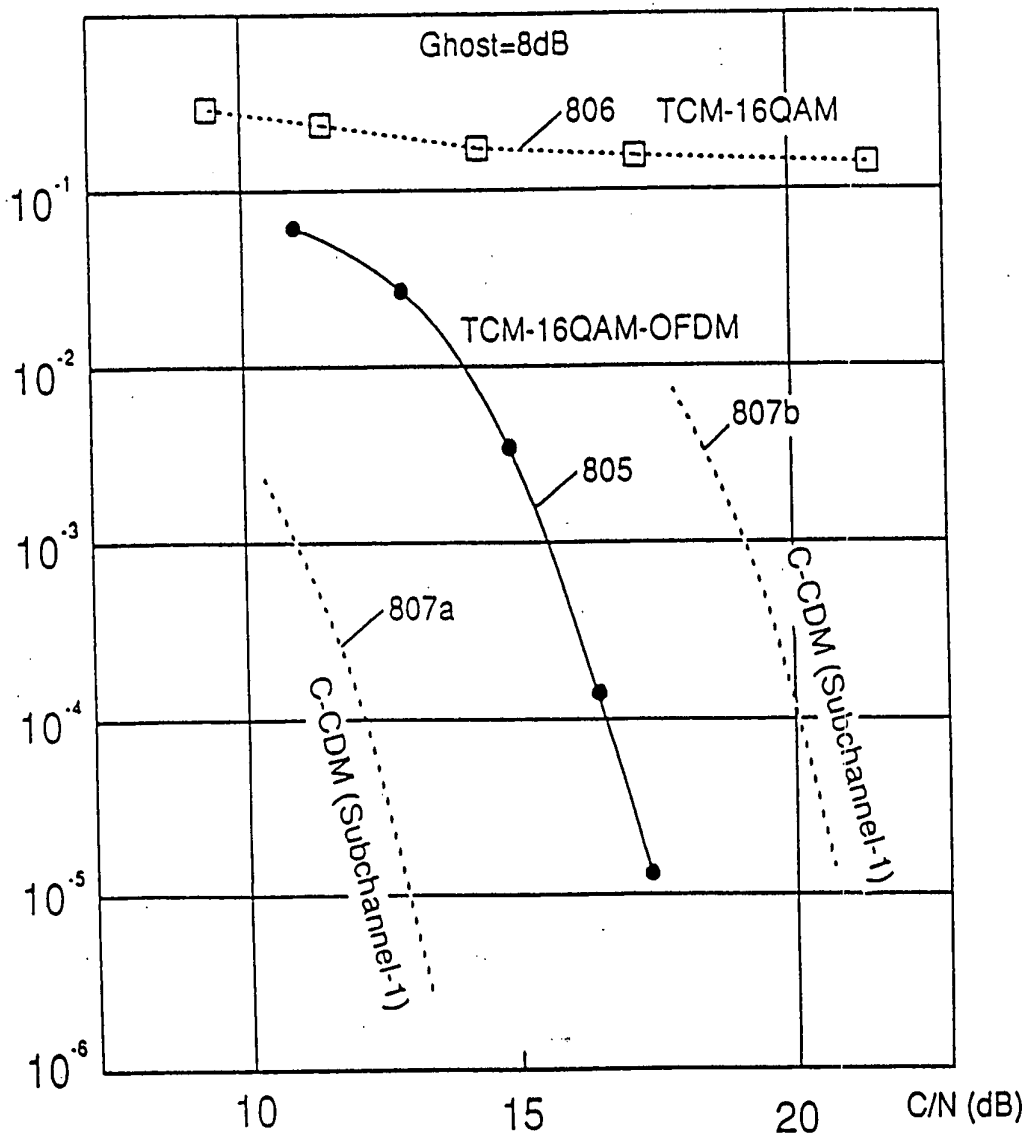

796a
Effective Symbol Period
797a
Guard Interval
796b
Effective Symbol Period
Guard Interval
ts
tg
ts
tg
Time
Magnitude
t

FIG. 130



GHOST DELAY=2us. D/U=8dB

Figure 8 Bit Error Rate Performance Under Single Ghost and Gaussian Noise (1)

FIG. 131

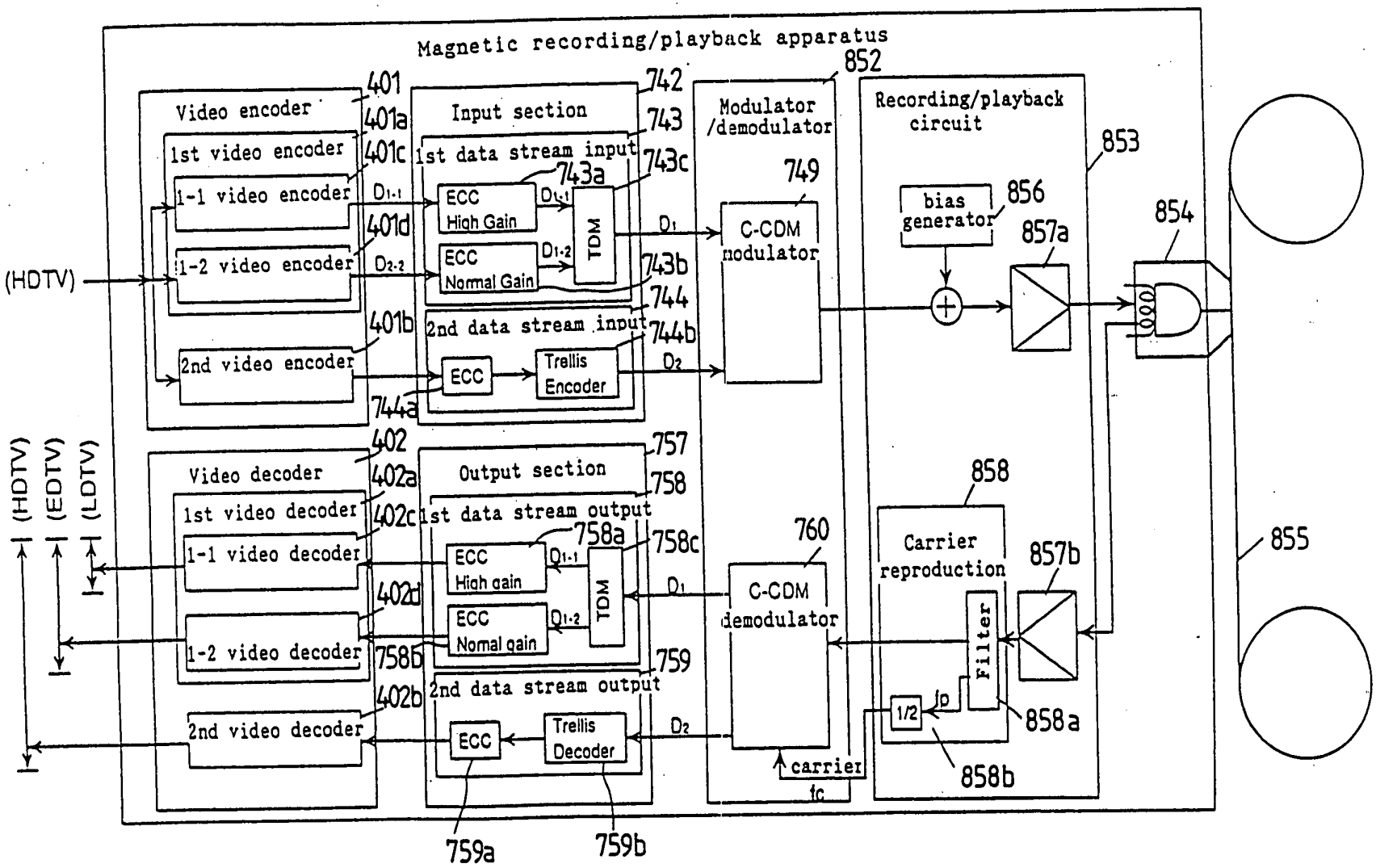

Magnetic recording/playback apparatus
Video encoder
401
401a
1st video encoder
401c
1-1 video encoder
D1-1
401d
1-2 video encoder
D2-2
401b
2nd video encoder
Input section
742
743
1st data stream input
743c
743a
ECC
High Gain
D1-1
TDM
D1
ECC
Normal Gain
D1-2
743b
744
2nd data stream input
744b
ECC
Trellis
Encoder
D2
744a
Modulator
/demodulator
852
749
C-CDM
modulator
Recording/playback
circuit
853
bias
generator
856
857a
854
(HDTV)
(HDTV)
(EDTV)
(LDTV)
Video decoder
402
402a
1st video decoder
402c
1-1 video decoder
402d
1-2 video decoder
758b
402b
2nd video decoder
Output section
757
758
1st data stream output
758a
758c
ECC
High gain
D1-1
TDM
D1
ECC
Normal gain
D1-2
759
2nd data stream output
ECC
Trellis
Decoder
D2
759a
759b
760
C-CDM
demodulator
carrier
fc
858
Carrier
reproduction
857b
Filter
1/2
fp
858a
858b
855

FIG. 132

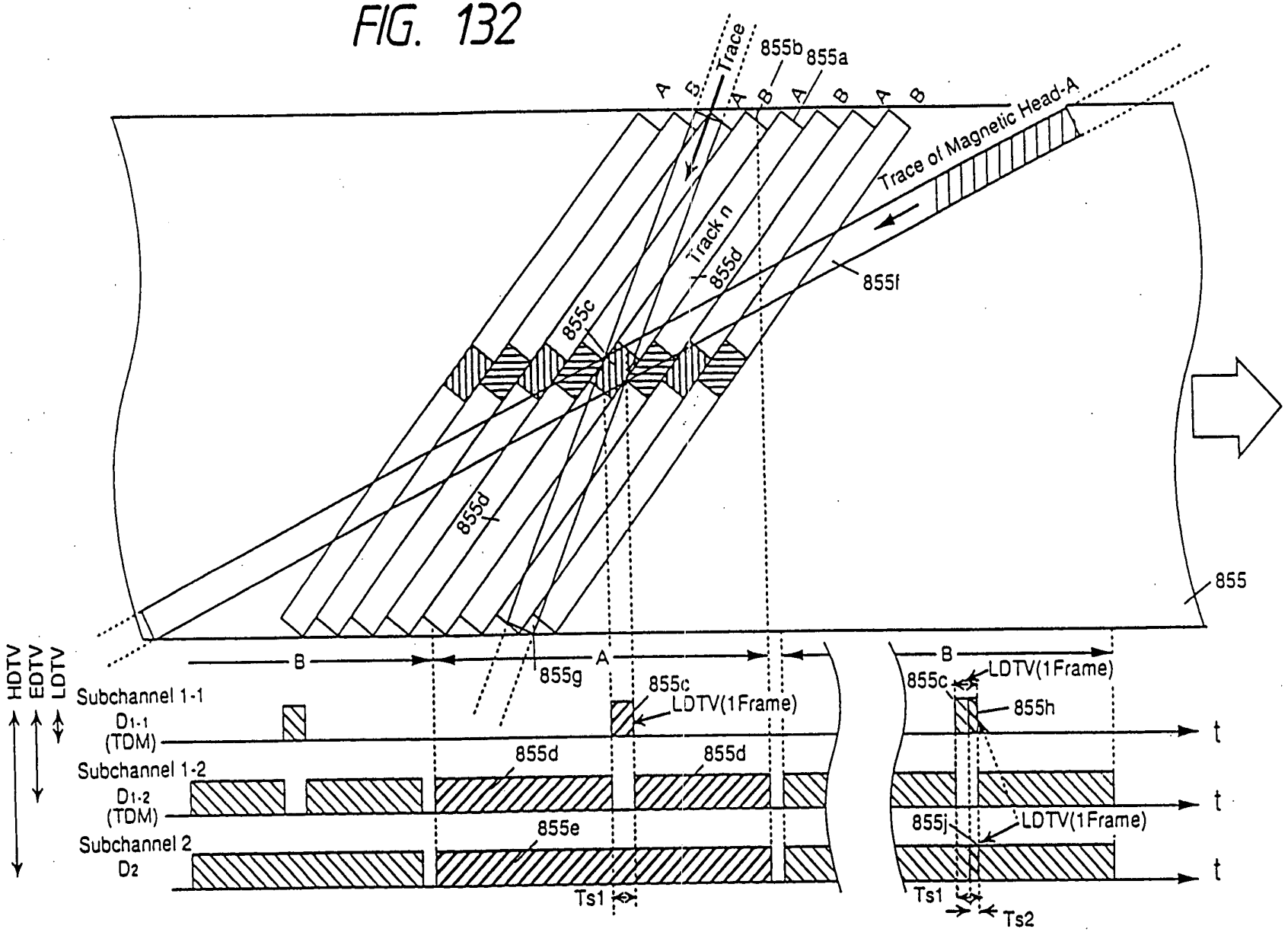

A
B
Trace
855b
855a
Trace of Magnetic Head-A
Track n
855d
855f
855c
855d
855
HDTV
EDTV
LDTV
B
A
855g
855c
LDTV(1Frame)
Subchannel 1-1
D1-1
(TDM)
855d
855d
Subchannel 1-2
D1-2
(TDM)
855e
Subchannel 2
D2
Ts1
B
LDTV(1Frame)
855c
855h
t
t
855j
LDTV(1Frame)
t
Ts1
Ts2

FIG. 133

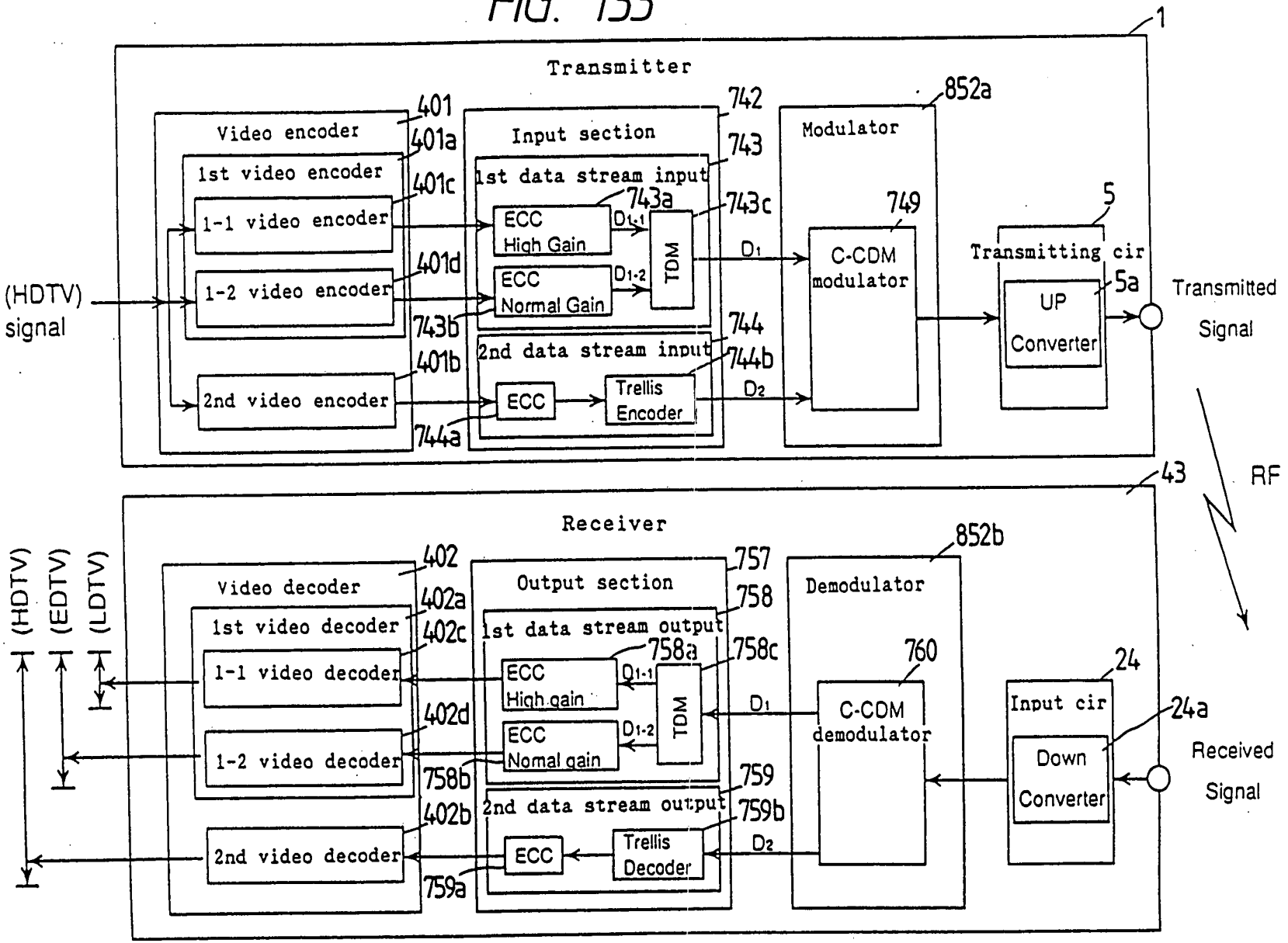

1
Transmitter
Video encoder
401
401a
1st video encoder
401c
1-1 video encoder
401d
1-2 video encoder
743b
401b
2nd video encoder
744a
Input section
742
743
1st data stream input
743a
ECC
High Gain
D1-1
743c
TDM
D1-2
ECC
Normal Gain
744
2nd data stream input
744b
ECC
Trellis
Encoder
D2
Modulator
852a
749
C-CDM
modulator
D1
5
Transmitting cir
UP
Converter
5a
(HDTV)
signal
Transmitted
Signal
RF
43
Receiver
(HDTV)
(EDTV)
(LDTV)
Video decoder
402
402a
1st video decoder
402c
1-1 video decoder
402d
1-2 video decoder
758b
402b
2nd video decoder
759a
Output section
757
758
1st data stream output
758a
ECC
High gain
D1-1
758c
TDM
D1-2
ECC
Nomal gain
759
2nd data stream output
759b
ECC
Trellis
Decoder
D2
Demodulator
852b
760
C-CDM
demodulator
D1
24
Input cir
Down
Converter
24a
Received
Signal

FIG. 134

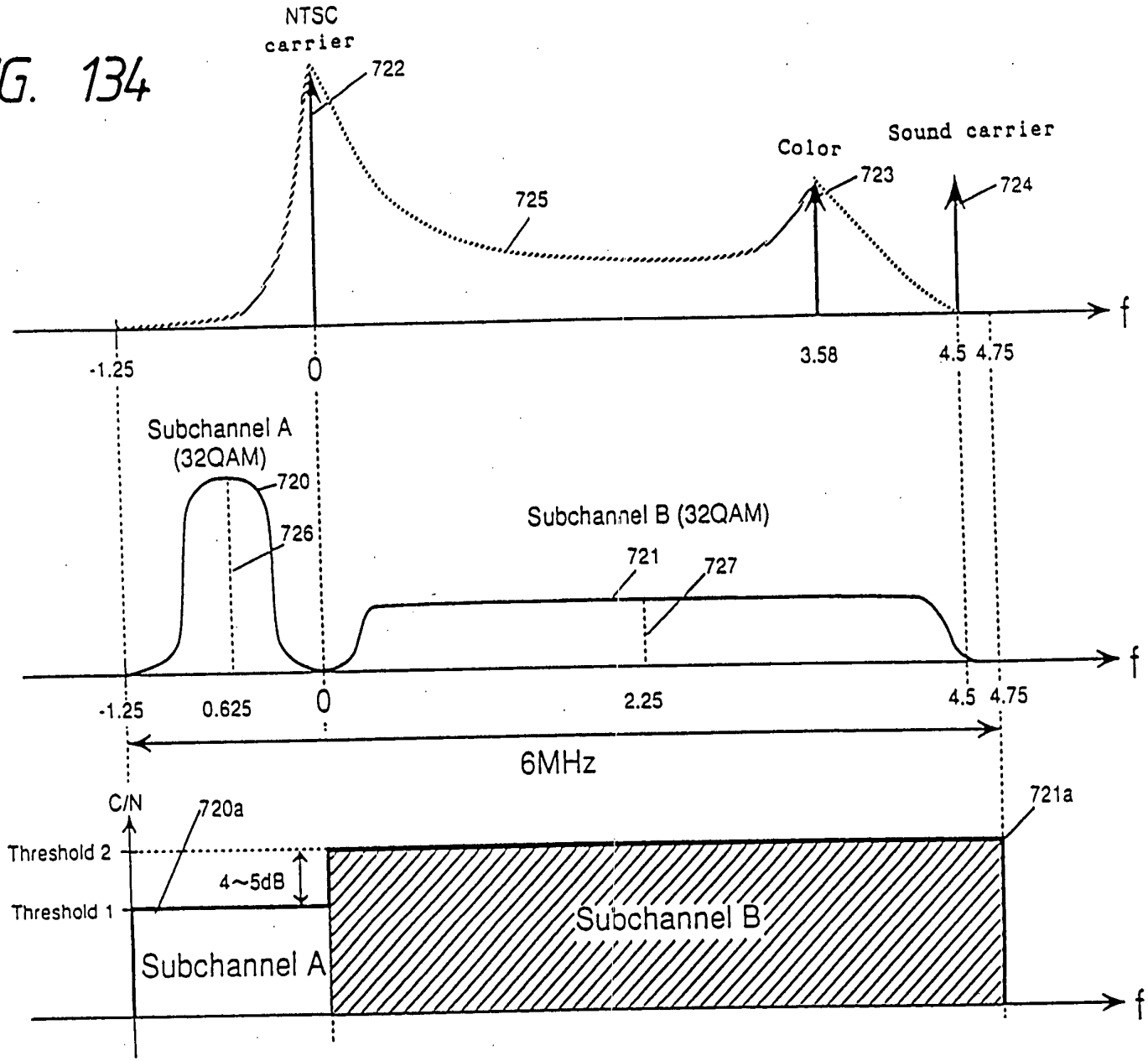

NTSC carrier
722
725
Color
723
Sound carrier
724
f
-1.25
0
3.58
4.5
4.75
Subchannel A (32QAM)
720
726
Subchannel B (32QAM)
721
727
f
-1.25
0.625
0
2.25
4.5
4.75
6MHz
C/N
720a
721a
Threshold 2
4~5dB
Threshold 1
Subchannel A
Subchannel B
f

FIG. 135

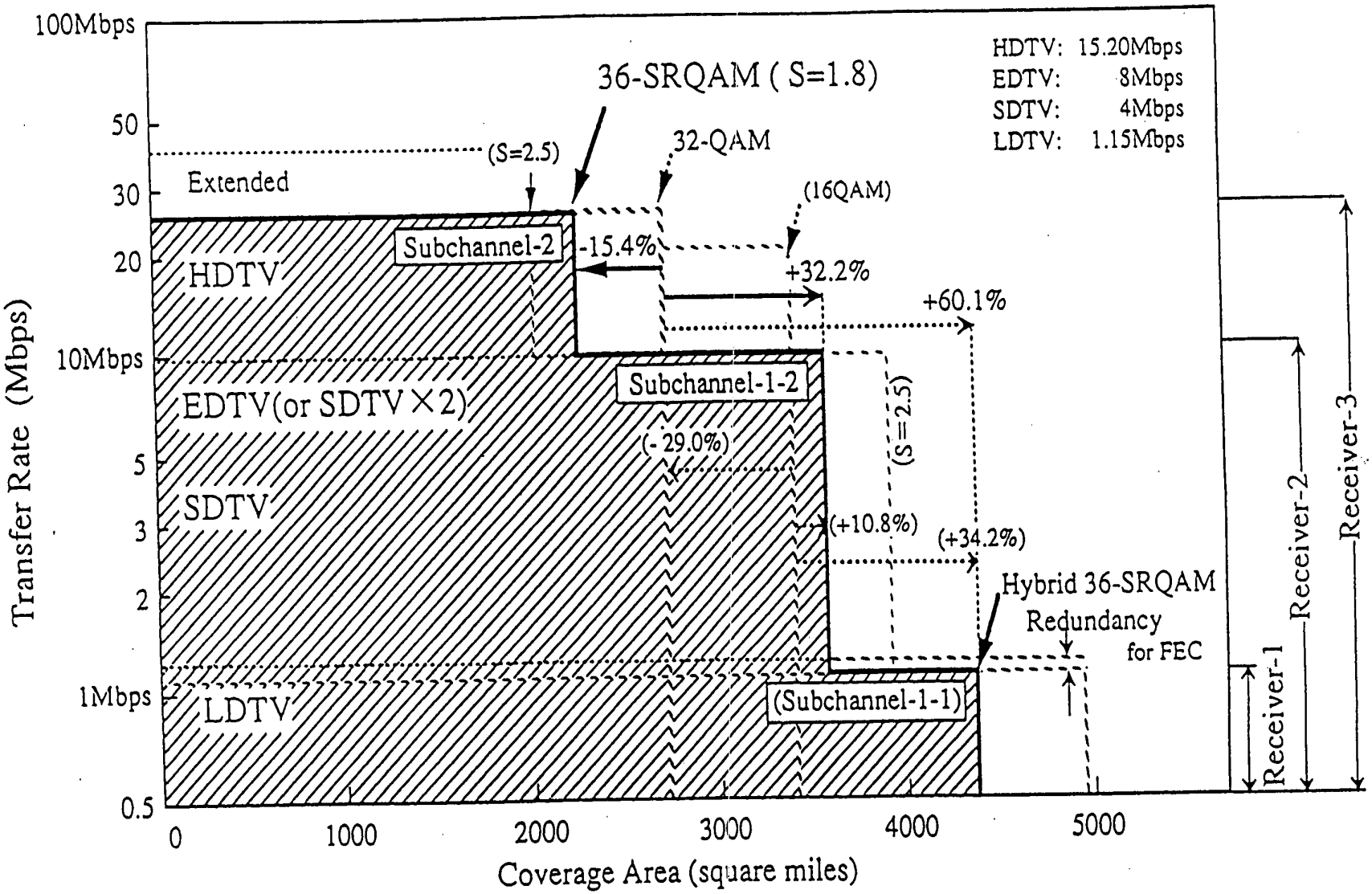

100Mbps
50
30
20
10Mbps
5
3
2
1Mbps
0.5
Transfer Rate (Mbps)
0
1000
2000
3000
4000
5000
Coverage Area (square miles)
HDTV: 15.20Mbps
EDTV: 8Mbps
SDTV: 4Mbps
LDTV: 1.15Mbps
36-SRQAM (S=1.8)
32-QAM
(16QAM)
(S=2.5)
Extended
Subchannel-2
HDTV
-15.4%
+32.2%
+60.1%
Subchannel-1-2
EDTV(or SDTV×2)
(- 29.0%)
(S=2.5)
SDTV
(+10.8%)
(+34.2%)
Hybrid 36-SRQAM
Redundancy
for FEC
(Subchannel-1-1)
LDTV
Receiver-1
Receiver-2
Receiver-3

FIG. 136

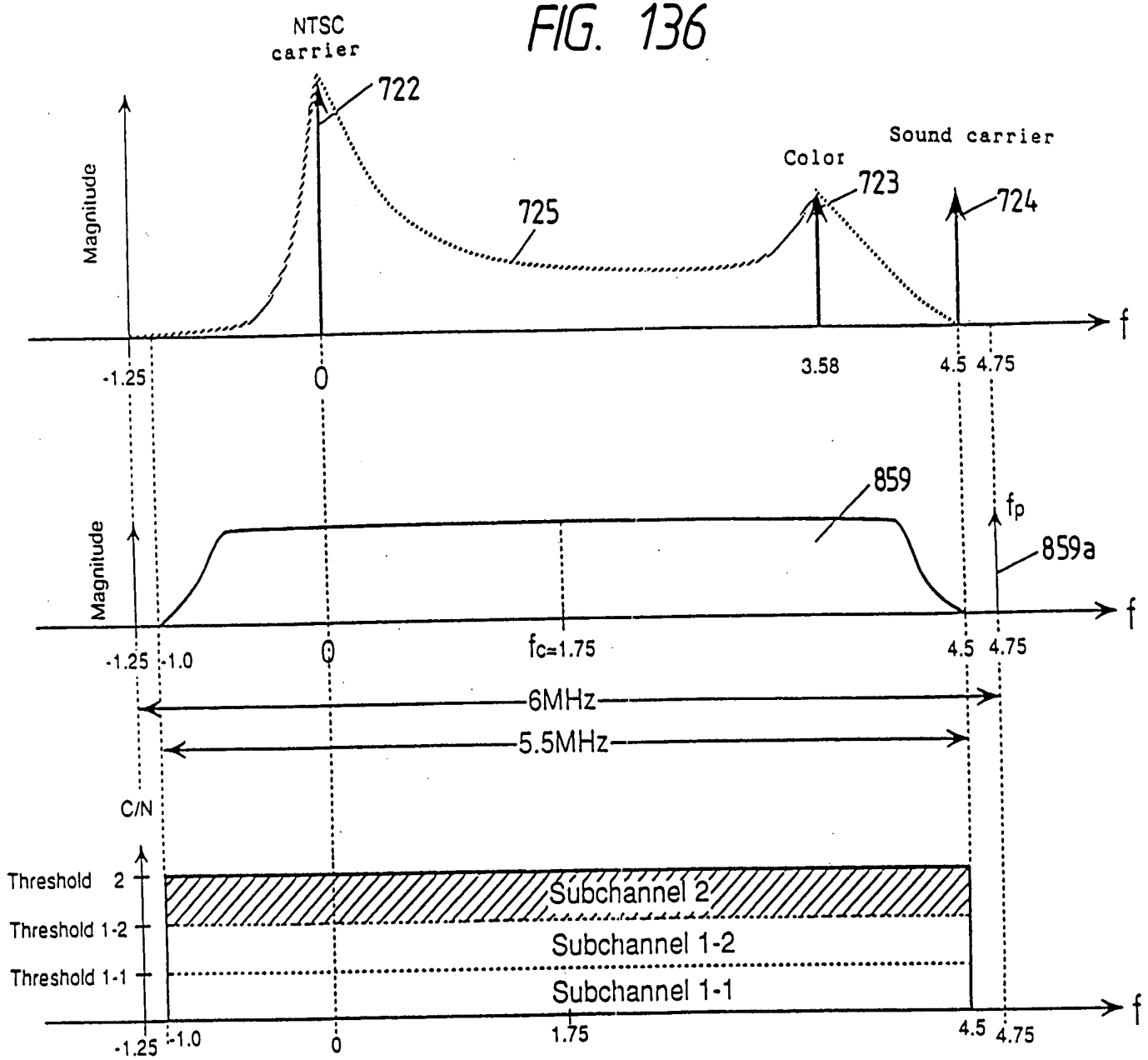

NTSC carrier
722
Sound carrier
Color
723
724
725
Magnitude
f
-1.25
0
3.58
4.5
4.75
859
fp
859a
fc=1.75
-1.0
6MHz
5.5MHz
C/N
Threshold 2
Threshold 1-2
Threshold 1-1
Subchannel 2
Subchannel 1-2
Subchannel 1-1
1.75

FIG. 137

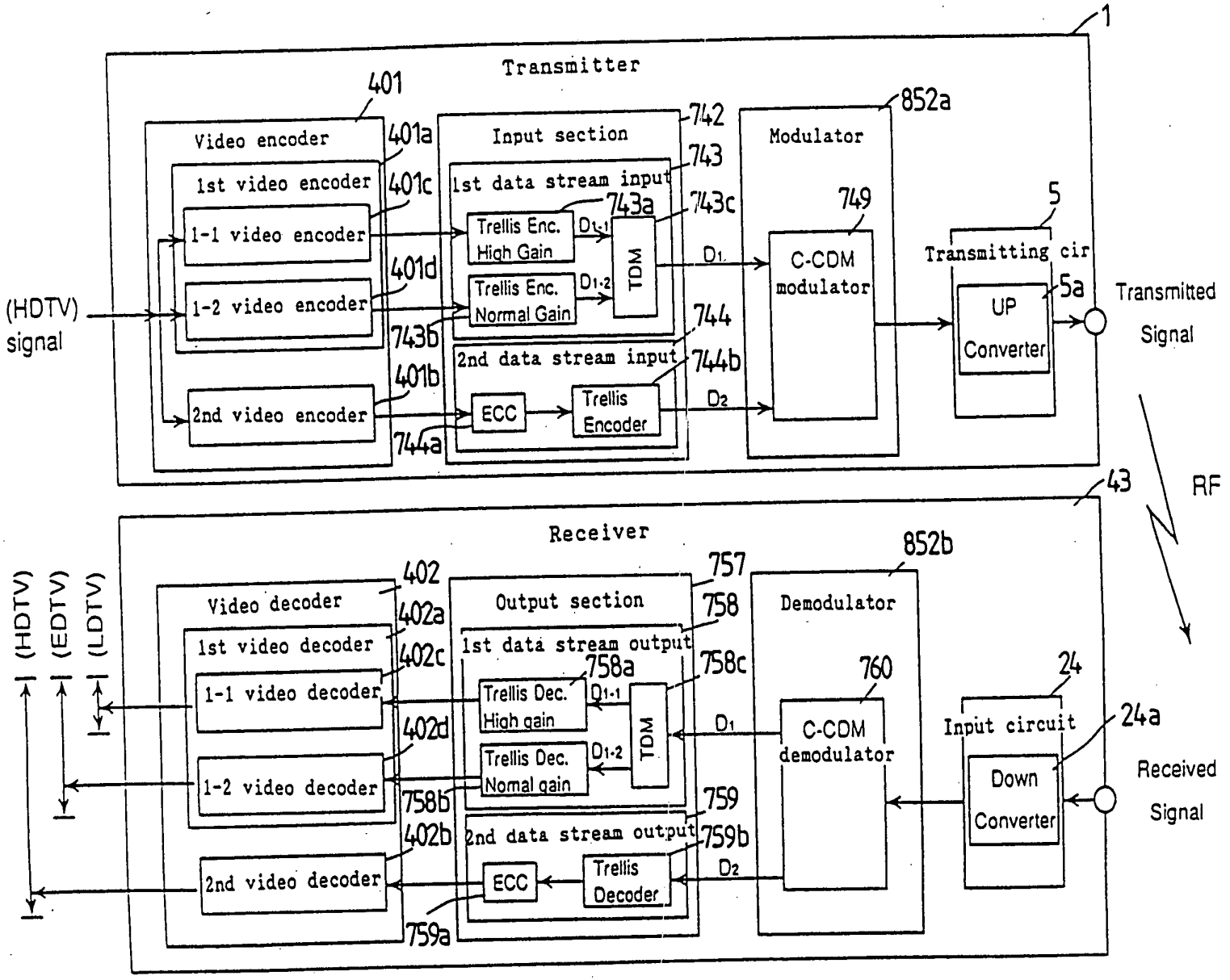
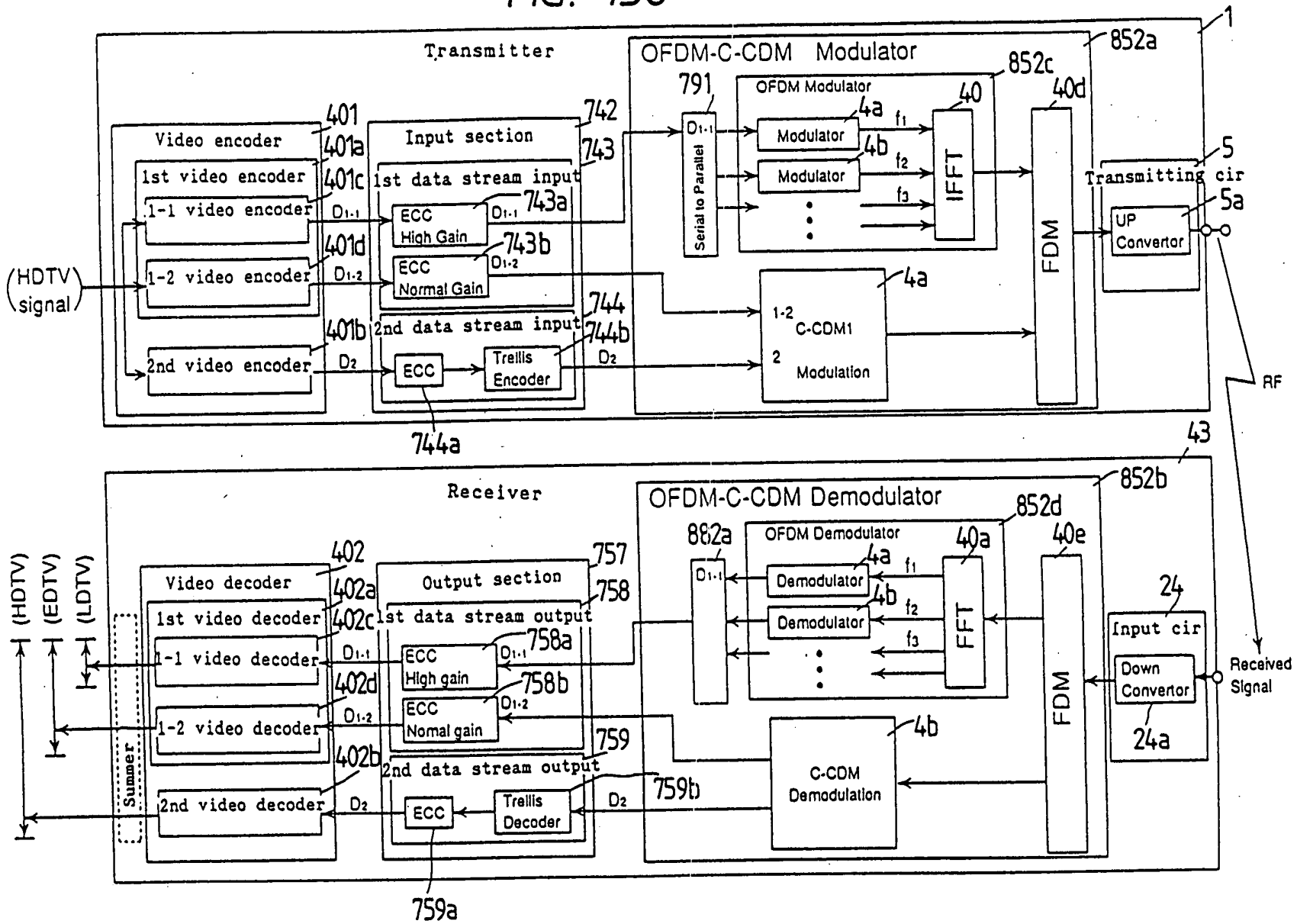

1
Transmitter
401
Video encoder
401a
1st video encoder
401c
1-1 video encoder
1-2 video encoder
401d
743b
401b
2nd video encoder
744a
742
Input section
743
1st data stream input
743a
Trellis Enc. High Gain
D1-1
743c
TDM
Trellis Enc. Normal Gain
D1-2
744
2nd data stream input
744b
ECC
Trellis Encoder
D2
852a
Modulator
749
C-CDM modulator
D1
5
Transmitting cir
5a
UP Converter
Transmitted Signal
(HDTV) signal
RF
43
Receiver
852b
(HDTV)
(EDTV)
(LDTV)
402
Video decoder
402a
1st video decoder
402c
1-1 video decoder
1-2 video decoder
402d
758b
402b
2nd video decoder
759a
757
Output section
758
1st data stream output
758a
Trellis Dec. High gain
D1-1
758c
TDM
Trellis Dec. Nomal gain
D1-2
759
2nd data stream output
759b
ECC
Trellis Decoder
D2
Demodulator
760
C-CDM demodulator
D1
24
Input circuit
24a
Down Converter
Received Signal

FIG. 138


Transmitter
OFDM-C-CDM Modulator
852a
1
852c
791
OFDM Modulator
40
40d
401
742
Video encoder
401a
Input section
743
1st video encoder
401c
1st data stream input
1-1 video encoder
D1-1
ECC
High Gain
743a
Serial to Parallel
Modulator
4a
f1
IFFT
FDM
5
Transmitting cir
401d
743b
1-2 video encoder
D1-2
ECC
Normal Gain
Modulator
4b
f2
f3
UP
Convertor
5a
(HDTV)
signal
744
2nd data stream input
744b
401b
2nd video encoder
D2
ECC
Trellis
Encoder
1-2
C-CDM1
2
Modulation
4a
744a
RF
43
Receiver
OFDM-C-CDM Demodulator
852b
852d
882a
OFDM Demodulator
40a
40e
402
757
Video decoder
Output section
402a
758
1st video decoder
1st data stream output
402c
758a
1-1 video decoder
D1-1
ECC
High gain
Demodulator
4a
f1
FFT
FDM
24
Input cir
Down
Convertor
Received
Signal
(HDTV)
(EDTV)
(LDTV)
758b
402d
1-2 video decoder
D1-2
ECC
Nomal gain
Demodulator
4b
f2
f3
24a
Summer
759
402b
2nd data stream output
759b
2nd video decoder
D2
ECC
Trellis
Decoder
C-CDM
Demodulation
4b
759a

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